

Skylake-LP/H - Intel® Management Engine Firmware 11.0

Consumer Firmware Bring Up Guide

June 2015

Revision 1.0 - Production Version

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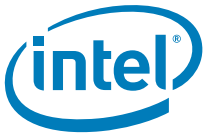
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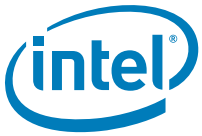


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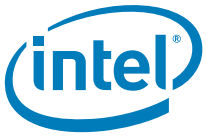
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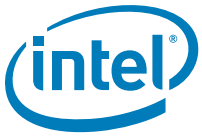
Revision	Description	Date
11.0.0.1080	Pre-Alpha Release: See change bars on the left side of the page.	September 2014
11.0.0.1100	Alpha Release: See change bars on the left side of the page.	December 2014
11.0.0.1106	ICC table additions: See change bars on the left side of the page.	January 2015
11.0.0.11xx	General table additions: See change bars on the left side of the page for specific page change. • Updated Table of Contents, List of Figures, and List of Tables to align with table content shifts for added items • Page 28 - Updated screen shot to reflect tool update • Page 40, 41 added missing table values • Page 50 - Removed frequency values that were not valid • Page 78 - 89 - Table contents were shifted to allow for table additions • Page 94 - Help text was added for CPU strap settings	February 2015
11.0.0.11xx	Updates made to reflect changes in ME kit package contents in Chapter 1 and visual changes in CPU Strap section in Chapter 2.	March 2015
11.0.0.1122	Beta Release: Table updates made, see change bars on left side of the page for location • Updated Table of Contents, List of Figures, and List of Tables to align with table content shifts for added items • Appendix D - PTT table updated to ensure correct values • Added additional row to include region order in the build settings popup • Inserted EcRegion in Flash Layout section • Inserted EC Master Access in Flash Settings section • Inserted Post Manufacturing Lock to ME Kernel section • Intel® AMT Watchdog Automatic Reset Enabled added to screen shot and table under Intel® AMT section under Intel® AMT Configuration • Minimum removed as a choice for redirection privacy / security level • Inserted screen shot and table for Hash Key Configuration for Bootguard /ISH and removed OEM Public Key Hash from Boot Guard Configuration under Platform Protection section • Updated screen shot for USB3 Port Configuration under Flex I/O section • Added additional note for PCIe controllers for RST under Flex I/O section • Updated screen shots to show removal of USB_Wakeout#/GPD7 signal configuration from GPIO and Power sections • Updated ME Feature Pins under GPIO to reflect changes in UI layout • Removed Appendix E RVP CRB A Step configuration settings • Added Appendix after renumbering for ISH Public Key Information • Updated WLAN Microcode version for Snowfield Peak in Networking and Connectivity Section • Updated CPU Straps section to IMON disabled = 0x1	March 2015



Revision	Description	Date
11.0.0.1126	General Updates: Table updates made, see change bars on left side of the page for location • Updated Table of Contents, List of Figures, and List of Tables to align with table content shifts for added items • Updated kit content reference for BIOS and LAN version • ICC Table 2.8 settings - Remove SPT-H only enable option reference for CLKRUN LPC 0 and CLKRUN LPC 1 • ICC Table 2.8 removed options for SKL-U and SKL-Y GPIO settings that were not listed • Flash Settings > Flash Configuration changed screen shot to match fields displayed • Internal PCH Buses > PCH Timer Configuration - Added APWROK Timing back to table and updated screen shot • Debug > Intel® Trace Hub Technology - Added Unlock Token field to table and updated screen shot • Appendix B tables updated to differentiate between SPT-LP and SPT-H PCH configurations • Appendix F references added • Quad Output Read Enabled and Dual Output Read Enabled values changed. • Debug Override bit value tables added to description for pre-production and production silicon. • MCTPDevPortEC setting changed to value 0x02 and screen shot changed. • Change BSP setting to disabled under Boot Guard Configuration. • ICC Table 2.8 settings updated to reflect clock gating wait value changes, crystal oscillator description changes, and GPIO Pin Mappings. See change bar for specific locations. • Screen shots changed for added fields	April 2015

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Revision	Description	Date
11.0.0.1133	General Updates: Checked kit for updates to user interface • Updated BSP Initialization description in table 2-7 Boot Guard Configuration • Updated Flash Settings section, write and erase clock frequency to 48MHz • Updated Flex I/O Section, SKL-H column to match default settings	May 2015
11.0.0.1136	General Updates: Checked kit for updates to user interface • Updated Platform Protection > Content Protection screen shot and added associated new rows to table 2-7 section 1 • Added IDLM under Debug table 2-15 section 4 with screen shot	May 2015
11.0.0.1140	General Updates: Checked kit for updates to user interface • Updated Platform Protection > Content Protection screen shot and added associated new rows to table 2-7 section 1 • Updated master pages to resolve numbering issue • Removed conditional indicators from template for previous platforms and cleaned up document to only include corporate/consumer indicators • Changed table format to allow for future formatting to easier add Lewisburg features • Added Intel® Network Frame Forwarder section in Intel® ME Kernel section and reordered remaining graphics and numbers accordingly • Changed DCI Enabled to Yes • Debug Override Pre-Production Silicon Bit 0: timeout changed to 60 • HDCP Internal Display Port1 – 5K changed to none • Moved Note in content protection section to each HDCP section and made conditional to corporate • Flex I/O port settings updated for inconsistencies • BSP settings changed to enabled • MctpDevicePortEc set to 0x0 • Flash Settings Invalid Instructions changed to match current settings and internal sighting 225442 • Internal sighting 225139 - SataPCIeComboPort1 should be GPIO instead PCIe (or GbE) on RVP3 • Updated screen shot for PCH Timer Configuration • Internal sighting 5253614 - SKL-H USB3/PCIe Combo Port Mapping Typo • GT US Power Plane Topology updated for setting mismatch • Added general note to NFF section about some PCH not supporting enabling of this option • Updated screen shot for ME region that included added display fields for Chipset Initialization	June 2015



1 Introduction

This document covers the Intel® Management Engine Firmware (Intel® ME) 11.0 - Consumer Firmware bring up procedure. Intel® ME is tied to essential platform functionality — this dependency cannot be avoided for engineering reasons.

The bring up procedure primarily involves building a Serial Peripheral Interface (SPI) Flash image that will contain:

- **[required]** Descriptor region — Contains sizing information for all other SPI Flash image regions, SPI settings (including Vendor Specific Configuration - or VSCC - tables, SPI device parameters), and region access permissions.
- **[required]** BIOS region — Contains firmware for the processor (or host) and/or Embedded Controller (EC).
- **[required]** Intel® ME FW region — Contains firmware for the Intel® Management Engine.
- **[optional]** GbE region — Contains firmware for Intel LAN solution.

For more details on SPI Flash layout, see the document **Skylake-LP/H SPI Programming Guide** and Appendix A. Once the SPI Flash image is built, it will be programmed to the target based platform and the platform will be booted. This document also covers any tests and checks required to ensure that this boot process is successful and that Intel® ME Consumer FW is operating as expected.

1.1 Related Documentation

VIP: Kit# 106913 - Intel® Ethernet Network Connections (20.1 OEM Gen) - LAN Software Production Candidate 20.1

1.2 Intel® ME FW Features

This firmware release includes the following applications:

- Platform Clocks – Tune clock silicon to the parameters of a specific board, configure clocks at run time, and power management clocks. **Benefit:** Allows extensive customizability and soft control of “Third generation” clock solution and makes clocks available before CPU powers up.
- Silicon Workaround Capability – Intel® ME FW will have limited capabilities to perform targeted workarounds for silicon issues. **Benefit:** Allows Intel® ME FW to address some issues that otherwise would require a new silicon stepping.

1.3 Prerequisites

Before this document is read and utilized, it is essential that the reader first review the Consumer FW Release Notes (included with this Intel® ME Consumer FW kit).

This document is constructed so that the reader can complete the bring up steps as given for the Intel Customer Reference Board (CRB). However, in the case that bring up is being performed on a different Intel® x based platform, this document will highlight any changes that must be imposed onto the bring up steps accordingly.

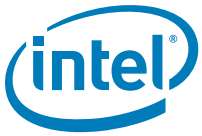
This document makes only the following limited assumptions regarding hardware:

- The platform is Intel® Skylake LP/H Chipset Family based
- The platform is equipped with one or more SPI Flash devices with a total capacity sufficient for storing all relevant firmware images.

1.4 Acronyms and Definitions

1.4.1 General

Acronym or Term	Definition
BIOS	Basic Input Output System
DIMM	Dual In-line Memory Module
DMI	Direct Media Interface
EC	Embedded Controller
FPF	Field Programmable Fuses
FW	Firmware
GbE	Gigabit Ethernet
HECI	Host Embedded Controller Interface (aka Intel® MEI)
Intel® ICCS	Intel® Integrated Clock Controller Service
Intel® ME	Intel® Management Engine (Intel®ME)
Intel® MEI	Intel® Management Engine Interface (Intel® MEI) (renamed from HECI)
Intel® PTT	Intel® Platform Trusted Technology (Intel® PPT)
Intel® MSS	Intel® Management and Security Status Application
KVM	Keyboard, Video, Mouse
LAN	Local Area Network
MCP	Multi-Chip Package (Central Processing Unit / Platform Controller Hub)
NVM	Non-Volatile Memory
OOB	Out-of-Band
OS	Operating System
PAVP	Protected Audio and Video Path
PCI	Peripheral Component Interconnect
PCIe*	Peripheral Component Interconnect Express
PHY	Physical Layer (Networking)
RTC	Real Time Clock
SBT	Intel® Small Business Technology
SMBus	System Management Bus
SPI Flash	Serial Peripheral Interface Flash
TPM	Trusted Platform Module
VSCC	Vendor Specific Configuration



1.4.2 Intel® Management Engine

Acronym or Term	Definition
3PDS	3rd Party Data Storage
Agent	Software that runs on a client PC with OS running
End User	The person who uses the computer (either Desktop or Mobile). In corporate, the user usually does not have administrator privileges.
Host or Host CPU	The processor that is running the operating system. This is different than the management processor running the Intel® Management Engine Firmware.
Host Service/Application	An application that is running on the host CPU
INF	An information file (.inf) used by Microsoft* operating systems that supports the Plug & Play feature. When installing a driver, this file provides the OS the necessary information about driver filenames, driver components, and supported hardware.
Intel® Management Engine Interface (Intel® MEI)	Interface between the Management Engine and the Host system
Intel® MEI driver	Intel® ME host driver that runs on the host and interfaces between ISV Agents and the Intel® ME HW.
IT User	Information Technology User. Typically very technical and uses a management console to ensure functionality of multiple PCs on a network.
LMS	Local Management Service: A SW application which runs on the host machine and provide a secured communication between the ISV agent and the Intel® Management Engine Firmware.
Intel® ME	Intel® Management Engine: The embedded processor residing in the chipset MCP
MECI	ME-VE Communication Interface
NVM	Non-Volatile Memory: A type of memory that will retain its contents even if power is removed. In the Intel® AMT current implementation, this is achieved using a FLASH memory device.
OOB Interface	Out Of Band interface: This is WSMAN interface over secure or non-secure TCP protocol.
OS not Functional	The Host OS is considered non-functional in Sx power state and any one of the following cases when system is in S0 power state: • OS is hung • After PCI reset • OS watch dog expires • OS is not present
System States	Operating System power states such as S0. See detailed definitions in System States and Power Management section.

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1.4.3 System States and Power Management

Acronym or Term	Definition
G3	A system state of Mechanical Off where all power is disconnected from the system. G3 power state does not necessarily indicate that RTC power is removed.
CM0	Intel® Management Engine firmware power state where all hardware power planes are activated. The host power state is S0.
CM3	Intel® Management Engine power state where the host is in Sx. The processor DRAM Controller is turned off and DRAM power stays in off/ self refresh mode. There is no UMA usage in CM3 state. Less than 1MB of SRAM used for code and data. Code is executed off of flash takes ~1mS.
CM0-PG	Core Well Powered; Intel® ME Well Powered; (Intel® ME core not consuming power) DRAM available.
CM3-PG	An Intel® ME Firmware power state where no power is applied to the Management Engine subsystem. (Intel® ME firmware is shut down).
OS Hibernate	System state where the OS state is saved on the hard drive.
S0	A system state where power is applied to all HW devices and the system is running normally.
S1, S2, S3	A system state where the host CPU is halted but power remains available to the memory system (memory is in self-refresh mode).
S4	A system state where the host CPU and memory are not active.
S5	A system state where all power to the host system is off, however the power cord (and/or battery in mobile designs) is still connected.
Shut Down	Equivalent to the S5 state.
Snooze Mode	Intel® Management Engine activities are mostly suspended to save power. The Intel® Management Engine monitors HW activities and can restore its activities depending on the HW event.
Standby	System state where the OS state is saved in memory and resumed from the memory when mouse/keyboard is clicked.
Sx	All S states which are different than S0.

1.5 Reference Documents

Document	Doc Number/ Location*
Skylake Intel® Management Engine (Intel® ME) and Embedded Controller Interaction Product Specification Revision 0.5	549024 / CDI
Intel® Management Engine BIOS Writers Guide	TBD / *
Intel® Management Engine (Intel® ME) 11 SKU Firmware Consumer *Compliance Guide for Skylake PCH-H/LP Chipset Family - Skylake Platform Compliancy and Testing Guide - Revision 1.1*	547408/ CDI

Note: * Unless specified otherwise, a document can be ordered by providing its reference number to your Intel Field Applications Engineer.

1.6 Format and Notation

The formats and notations used within this document model are those typically used by BIOS vendors. This section describes the formatting and the notations that will be followed in this document.

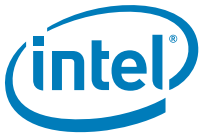


Table 1-1. Number Format Notation

Number Format	Notation	Example
Decimal (default)	d	14d. Note that any number without an explicit suffix can be assumed to be decimal.
Binary	b	1110b
Hex	h	0Eh
Hex	0x	0x0E

Table 1-2. Data Format Notation

Data Type	Notation	Size
Bit	b	Smallest unit, 0 or 1
Byte	B	8 bits
Word	W	16 bits or 2 bytes
Double-word	DW	32 bits or 4 bytes
Quad-word	QW	8 bytes or 4 words
Kilobyte	KB	1024 bytes
Megabit	Mb	1,048,576 bits or 128 KB
Megabyte	MB	1,048,576 bytes or 1024 KB
Gigabit	Gb	1,073,741,824 bits
Gigabyte	GB	1024 MB

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1.7 Kit Contents

The Intel® ME Consumer FW kit can be downloaded from VIP (https://platformsw.intel.com/). The contents of this kit are detailed below (Note that only key files are listed).

Table 1-3. Kit Contents (Sheet 1 of 4)

File or [Directory]	Content Description
[root]	Root directory
SPT Consumer FW Bring Up Guide.pdf	This document
Skylake-H Client SPI Programming Guide.pdf	How to program SPI device parameters and descriptor region details. Also contains a complete SPI Flash softstrap reference.
Skylake-LP/H Client SPI Programming Guide.pdf	How to program SPI device parameters and descriptor region details. Also contains a complete SPI Flash softstrap reference.
[Image Components]	
[BIOS]	
PreProduction_SKLX085_0184_02_RomImages_ReleaseBuild.rom	BIOS image only for Intel CRB.
Production_SKLX085_0184_02_RomImages_ReleaseBuild.rom	BIOS image only for Intel CRB.
[GbE]	
n7_spt_h_lm_non_lan_sw_0.8.bin	Intel® LAN PHY LPT-H firmware image.
n7_spt_lp_lm_non_lan_sw_1.3.bin	Intel® LAN PHY LPT-LP firmware image.
[ME]	
ME_11.0_Consumer_C0_H.bin	Intel® ME firmware image (**Non Production FW**) - supports **unfused** Skylake PCH-LP Platform I/O MCP steppings: • Unfused (Super SKU) **Note: For PAVP Testing**, you must match Production FW with Production Part and Non Production FW with Non Production Parts.
ME_11.0_Consumer_D0_H_Production.bin	
[Installers]	
Intel®_ME SW Installation Guide.pdf	Intel® ME Software installation Guide.
[ME_SW_MSI]	
IntelMEFWVer.dll	
MUP	XML file
SetupME	
WixLicenseNote.txt	
[MEI-Only Installer MSI]	
IntelMEFWVer.dll	
MEISetup	
MUP	XML file
[Tools]	
[ICC_Tools]	

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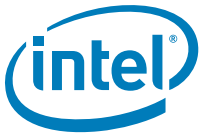


Table 1-3. Kit Contents (Sheet 2 of 4)

File or [Directory]	Content Description
Intel® ME Firmware Integrated Clock Control (ICC) Tools User Guide.pdf	ICC Tools User Guide
[CCT]	
cct	Exe file
cct	Ini file
cctDll.dll	
cctWin	Exe file
[EFI]	
cct.efi	CCT for EFI
[System Tools]	
Open Watcom Public License.pdf	Sybase Open Watcom Public License version 1.0 document.
System Tools User Guide.pdf	System Tools User Guide
[Flash Image Tool]	
fit.exe	Intel® Flash Image Tool (Intel® FIT)
newfiletmpl.xml	FITC Configuration XML file
vsccommn.bin	Binary containing the supported SPI parts
VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
[Flash Programming Tool]	
[DOS]	
fparts.txt	List of supported SPI Flash devices with specific Flash parameters
fpt.exe	Intel® FPT for DOS
[EFI64]	
fparts.txt	List of supported SPI Flash devices with specific Flash parameters
fpt.efi	Intel® FPT for EFI
[Windows]	
fparts.txt	List of supported SPI Flash devices with specific Flash parameters
fptw.exe	Intel® FPT for Windows*
Idrvdll.dll	
Pmxdll.dll	
[Windows64]	
fparts.txt	List of supported SPI Flash devices with specific Flash parameters
fptw64.exe	Intel® FPT for Windows* (64-bit) OS
Idrvdll32e.dll	
Pmxdll32e.dll	
[FWUpdate]	
[EFI64]	
FWUpdLcl.efi	FW Update Tool (EFI version)

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Table 1-3. Kit Contents (Sheet 3 of 4)

File or [Directory]	Content Description
[DOS]	
FWUpdLcl.exe	FW Update Tool (DOS version)
[Win]	
FWUpdLcl.exe	FW Update Tool (Windows* version 32bit)
[Win64]	
FWUpdLcl64.exe	FW Update Tool (Windows* version 64bit)
[Manifest Extension Utility]	
[Win]	
meu.exe	Intel® Manifest Extension Utility (MEU) executable file that allows input of FW binary and outputs and independent updatable partition that is compressed and signed.
[MEInfo]	
[DOS]	
MEInfo.exe	Intel® ME Information Tool (DOS version)
[EFI64]	
MEInfo.efi	Intel® ME Information Tool (EFI version)
[Windows]	
MEInfoWin.exe	Intel® ME Information Tool (Windows* version 32bit)
Idrvdll.dll	
Pmxdll.dll	
ISHLib.dll	
[Windows64]	
MEInfoWin64.exe	Intel® ME Information Tool (Windows* version 64bit)
Idrvdll32e.dll	
ISHLib.dll	
Pmxdll32e.dll	
[MEManuf]	
[DOS]	
MEManuf.exe	Intel® ME Manufacturing Tool (DOS version)
vsccommn.bin	Binary containing the supported SPI parts
VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
[EFI64]	
VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
MEManuf.efi	Intel® ME Manufacturing Tool (EFI version)
vsccommn.bin	Binary containing the supported SPI parts
[Windows]	
Idrvdll.dll	
MEManufWin.exe	Intel® ME Manufacturing Tool (Windows* version 32bit)

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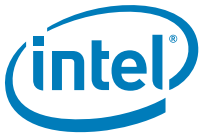


Table 1-3. Kit Contents (Sheet 4 of 4)

File or [Directory]	Content Description
Pmxdll.dll	
ISHLib.dll	
vsccommn.bin	Binary containing the supported SPI parts
VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
[Windows64]	
Idrvdll32e.dll	
ISHLib.dll	
MEManufWin64.exe	Intel® ME Manufacturing Tool (Windows* version 64bit)
Pmxdll32e.dll	
vsccommn.bin	Binary containing the supported SPI parts
VSCCommn_bin Content.pdf	Documentation listing the SPI parts supported by vscccommn.bin
(empty)	

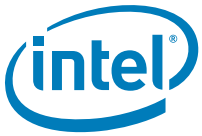
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1.8 External Hardware Requirements for Bring Up

Acquire the following hardware tools before moving on to the next step.

Windows* OS System	Flash Burner	DOS Bootable USB Key
		
Equipment: • Laptop or desktop that supports win32 applications **Purpose:** • Will run firmware image assembly and build process software.	**Equipment:** • (Optional) For platforms that don't boot, a Flash Chip Programmer will be required • For platforms that can boot to DOS or Windows*, a Intel® FPT is provided in this kit **Purpose:** • Will burn firmware images onto the target system Flash device(s).	**Equipment:** • A DOS Bootable USB Key (Size > 512 MB) **Purpose:** • Acting as a bootable device and will be used to run Intel® FPT (fpt.exe) directly on the system that is undergoing Bring Up process. • Or will be used to transfer a firmware image onto a Flash burner.

§ §



2 Image Creation: Intel® Flash Image Tool

Intel® Flash Image Tool (Intel® FIT) can be used to generate either a full SPI Flash binary image with Descriptor, GbE, BIOS, and Intel® ME Regions. Additionally, it can be used to create a simple image containing only the Intel® ME Region only for use with custom SPI Flash binary image assembly solutions. Use the steps shown in following sections.

After this image has been created, it will need to be burned onto the target platform's SPI Flash device(s). Section 3, "Programming SPI Flash Devices and Checking Firmware Status" later in this document provides steps to do this.

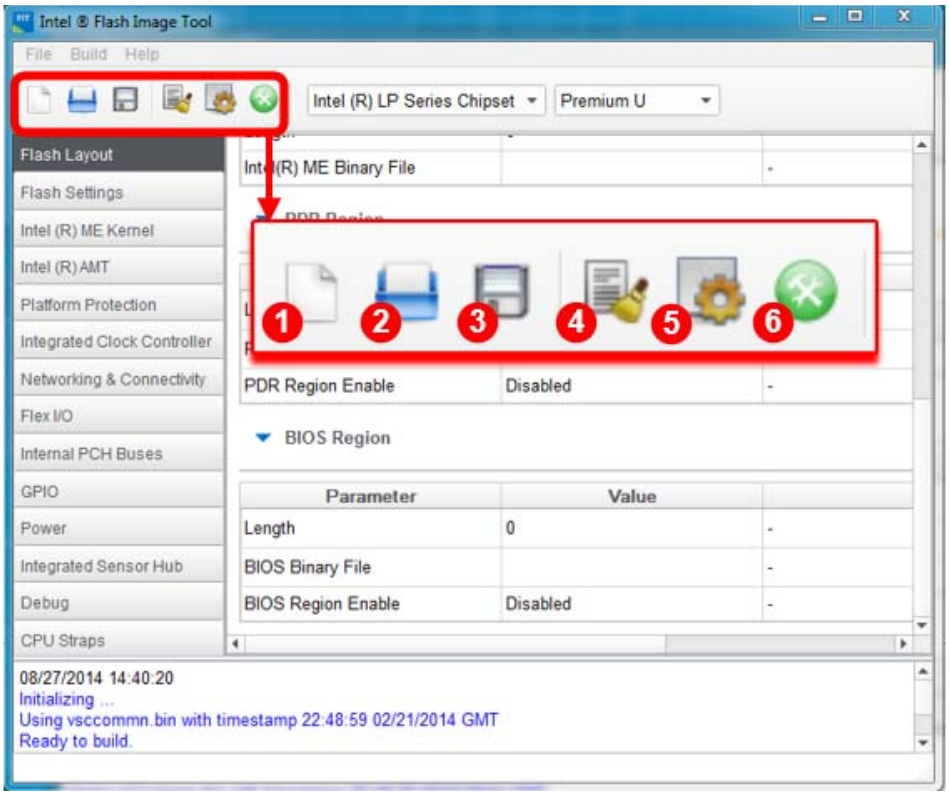
Note: The Flash Image Tool may be updated throughout the release cycles. As a general rule, please ensure you use the tools, images and other content from the same kit and refrain from using different version tools.

2.1 Start Intel®FIT

1. Invoke Intel® Flash Image Tool. Using Explorer*, navigate to **[root]\Tools\System Tools\Flash Image Tool**. Verify that the directory contents are correct (see Section 1.7). Double-click **FIT.exe**.
2. **NOTE:** In the tables below, where default settings are listed for SKL LP/H, if the value is the same one value will be listed. If there is a different default value when the program loads with either platform, both values will be listed to show the difference.

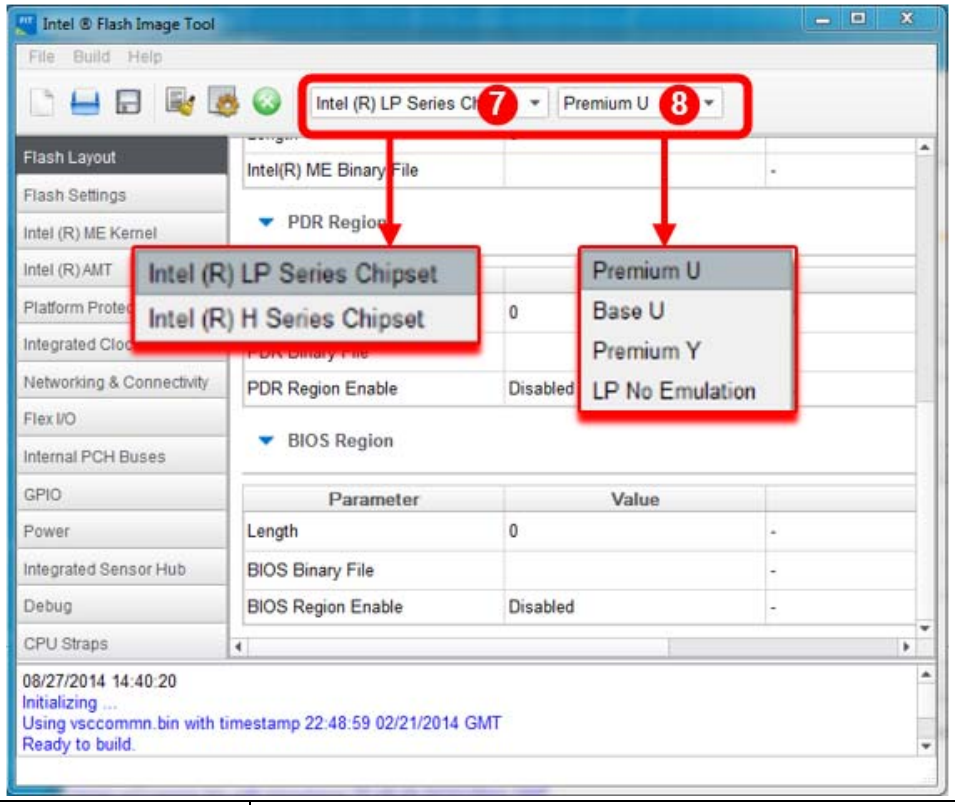
2.2 Step-by-Step Guide to Build SPI Flash Image with Intel® FIT Interface

Table 2-1. Intel® FIT - Initial Screen Layout (Sheet 1 of 7)

#	Label	Contents
		
1	**Button Interface**	This button labeled 'New' on rollover allows opening of a new session with default values
2	**Button Interface**	This button labeled 'Open' on rollover allows opening of an xml or bin file
3	**Button Interface**	This button labeled 'Save' on rollover allows saving of xml file
4	**Button Interface**	This button labeled 'Clear Console' clears the console area (see page 23)
5	**Button Interface**	This button labeled 'Build Settings' brings up the build settings popup Window see (Table 2-2)
6	**Button Interface**	This button labeled 'Build Image' on rollover allows build of the image

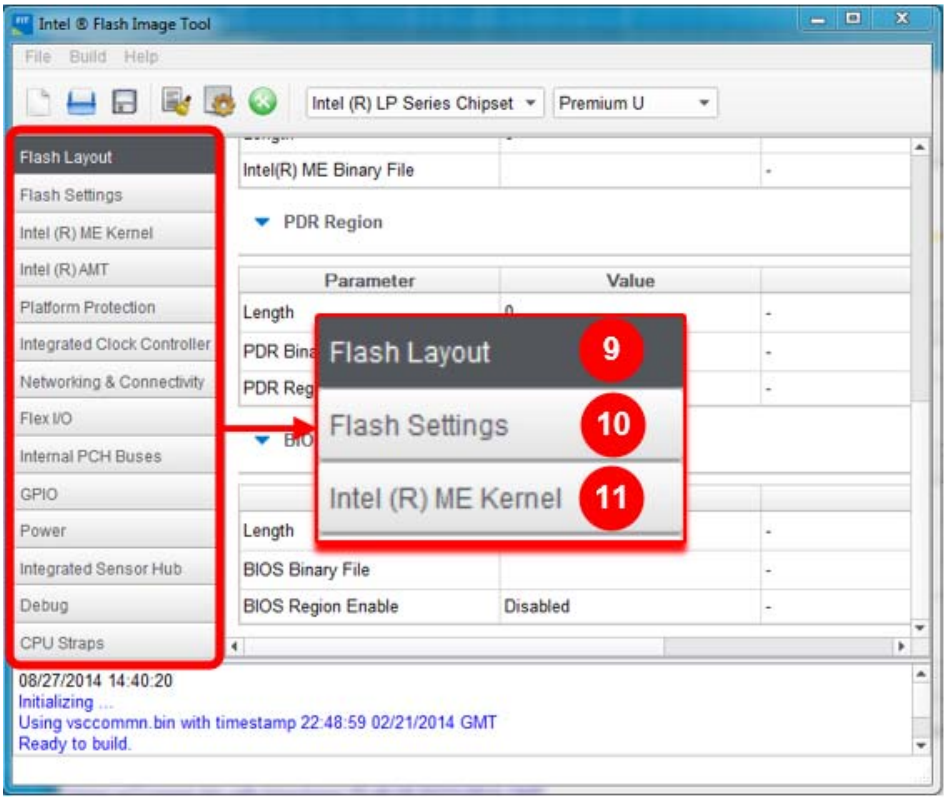
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Table 2-1. Intel® FIT - Initial Screen Layout (Sheet 2 of 7)

#	Label	Contents
		
7	**Drop Down Selector**	This drop down allows selection of platform
8	**Drop Down Selector**	This drop down allows selection of SKU within platform selected

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Table 2-1. Intel® FIT - Initial Screen Layout (Sheet 3 of 7)

#	Label	Contents
		

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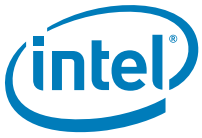


Table 2-1. Intel® FIT - Initial Screen Layout (Sheet 4 of 7)

#	Label	Contents
9	**Flash Layout Tab**	Flash Layout which contains (see Table 2-3): • Regions Descriptor Region GBE Region Intel® ME Region PDR Region EC Region BIOS Region
10	**Flash Settings Tab**	Flash Settings which contains (see Table 2-4): • Flash Components • Host CPU/ BIOS Master Access • Intel® ME Master Access • GBE Master Access • EC Master Access • Flash Configuration • VSCC Table - VSCC Entry • SPI based RPMC Configuration • BIOS Configuration
11	**Intel® ME Kernel Tab**	Intel® ME Kernel which contains (see Table 2-5): • Processor • Intel® ME Firmware Update • Intel® Services Configuration • Image Identification • MCTP Configuration • Firmware Diagnostics • Post Manufacturing Lock • Reserved

Table 2-1. Intel® FIT - Initial Screen Layout (Sheet 5 of 7)

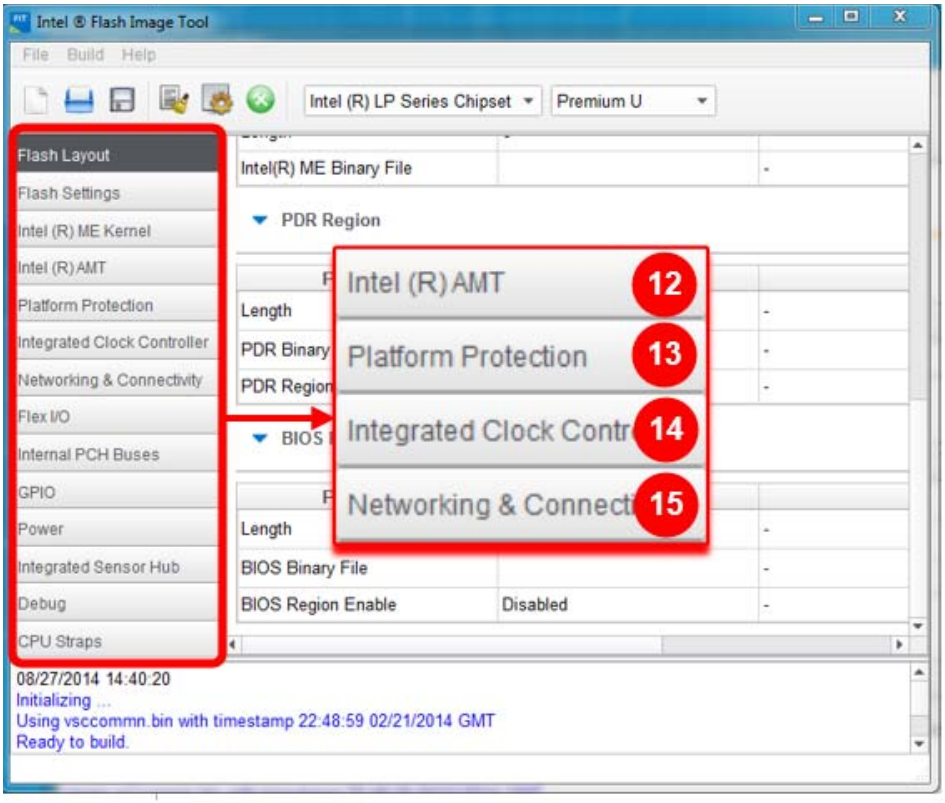
#	Label	Contents
		
12	**Intel® AMT Tab**	Intel® AMT which contains (see Table 2-6): • Intel® AMT Configuration • KVM Configuration • Provisioning Configuration • OEM Customizable Certificates (1, 2, 3) • OEM Default Certificates (1, 2, 3, 4, 5) • Redirection Configuration • TLS Configuration
13	**Platform Protection Tab**	Platform Protection which contains (see Table 2-7): • Content Protection • Graphics uController • Hash Key Configuration for Bootguard / ISH • Boot Guard Configuration • Intel® PTT Configuration • TPM Over SPI Bus Configuration
14	**Integrated Clock Controller Tab**	Integrated Clock Controller which contains (see Table 2-8): • Integrated Clock Controller Policies • Profiles
15	**Networking & Connectivity Tab**	Networking & Connectivity which contains (see Table 2-9): • Wired LAN Configuration • Wireless LAN Configuration • Intel® NFC Configuration

Table 2-1. Intel® FIT - Initial Screen Layout (Sheet 6 of 7)

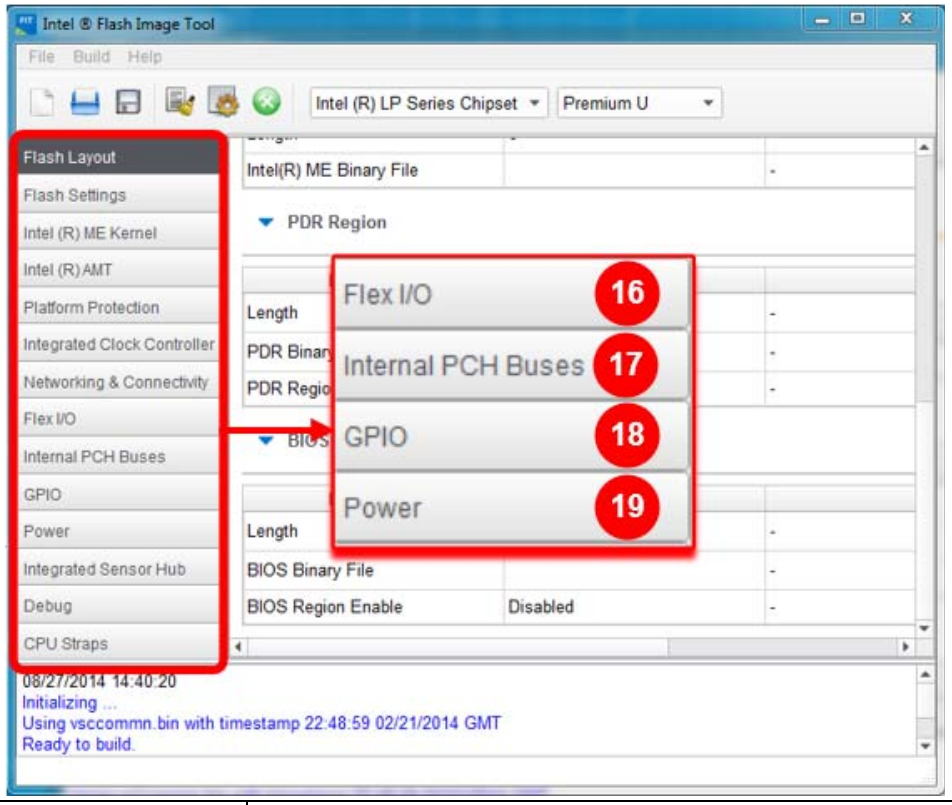
#	Label	Contents
		
16	**Flex I/O Tab**	Flex I/O which contains (see Table 2-10): • Intel® RST for PCIe Configuration • PCIe Lane Reversal Configuration • PCIe Port Configuration • SATA / PCIe Combo Port Configuration • SATA / PCIe Combo Port Select Polarity • USB3 Port Configuration • XHCI Port Configuration
17	**Internal PCH Buses Tab**	Internal PCH Buses which contains (see Table 2-11): • OPI Configuration • DMI Configuration • eSPI Configuration • PCH Timer Configuration • SMBus / SMLink Configuration
18	**GPIO Tab**	GPIO which contains (see Table 2-12): • LAN / GPIO Select • WLAN / GPIO Select • Platform Power / GPIO • ME Feature Pins
19	**Power Tab**	Power which contains (see Table 2-13): • Platform Power • Intel® ME Power Configuration • Deep Sx

Table 2-1. Intel® FIT - Initial Screen Layout (Sheet 7 of 7)

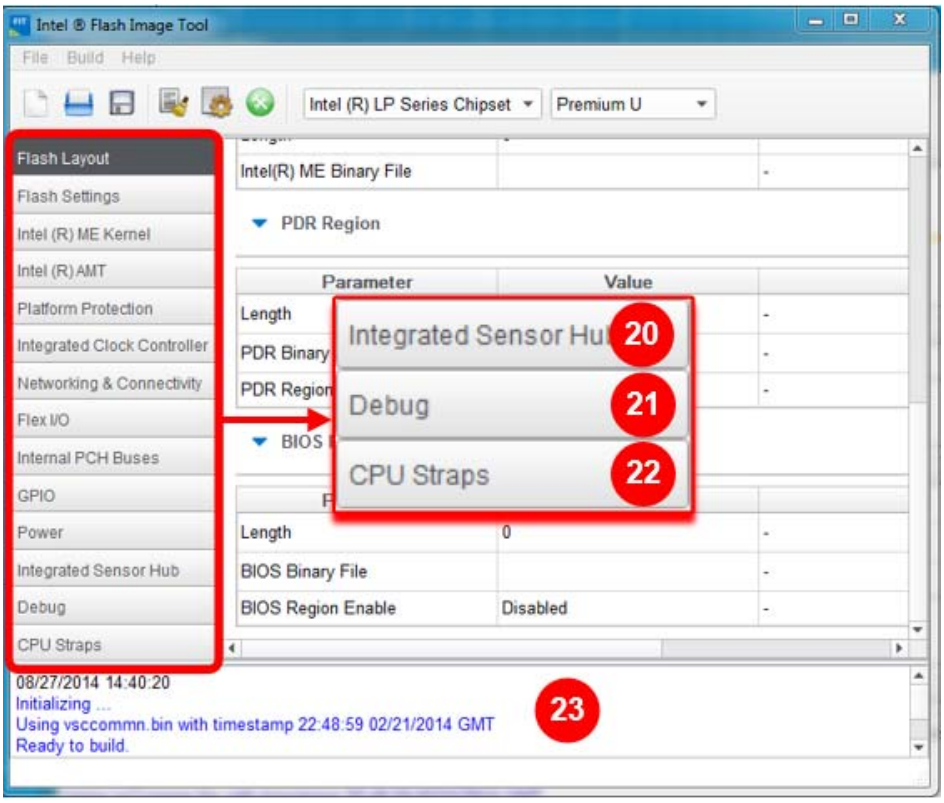
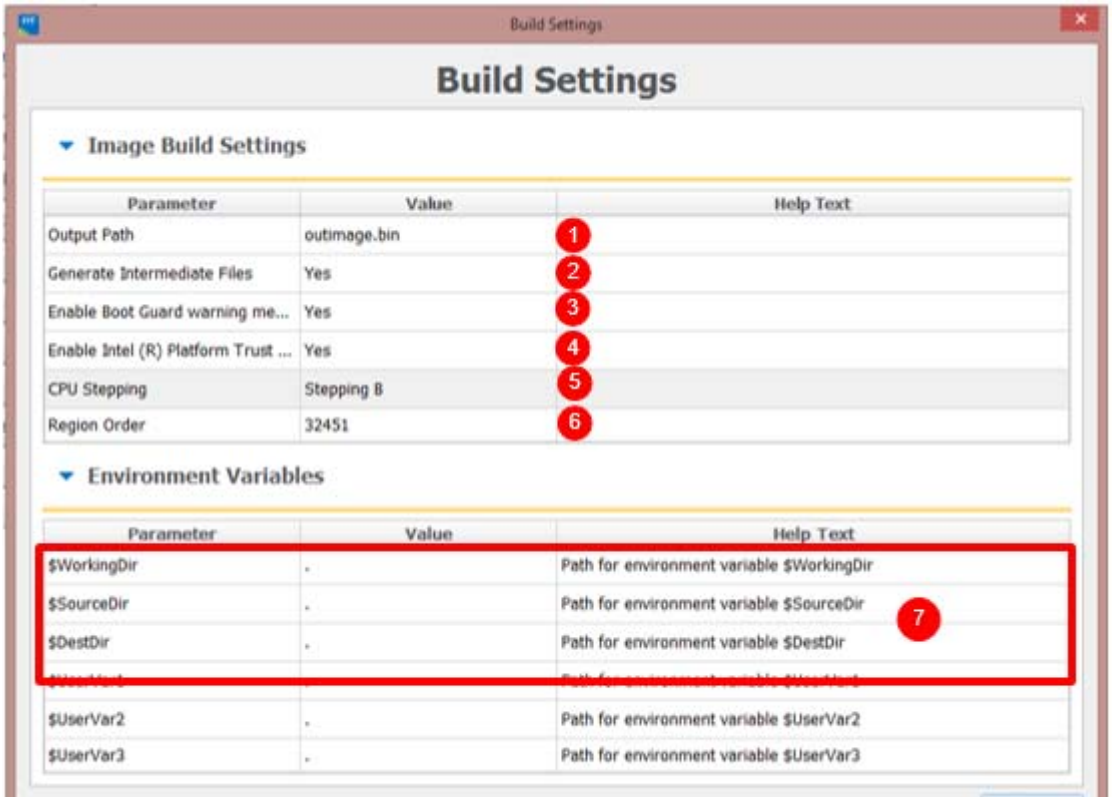
#	Label	Contents
		
20	**Integrated Sensor Hub Tab**	Integrated Sensor Hub which contains (see Table 2-14): • Integrated Sensor Hub • ISH Image • ISH Data
21	**Debug Tab**	Debug which contains (see Table 2-15): • Intel® ME Firmware Debugging Overrides • Direct Connection Interface Configuration • Intel® Trace Hub Technology
22	**CPU Straps Tab**	CPU Straps which contain a detailed list of parameters (see Table 2-16)
23	**Console Window Area**	Displays opening messages, log file entries, and build activity messages

Table 2-2. Intel® FIT - Build Settings (Sheet 1 of 2)

Click on Build Button in the top menu bar> Build Settings window pop up is displayed:



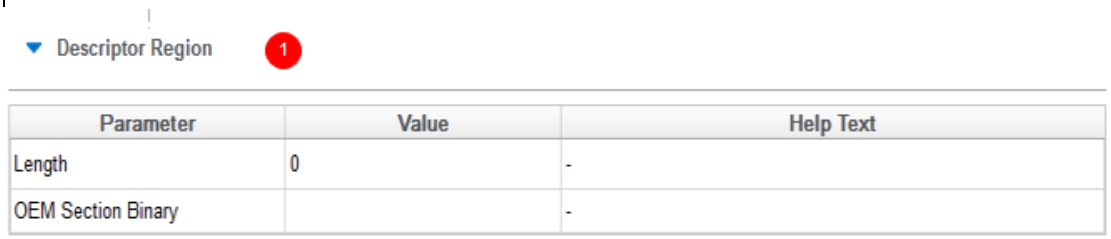
#	Parameter	CRB	Values
1	**Output Path**		Double click to the right of outimage.bin and click to get browse button to specify path and name of file to create for the build - default is outimage.bin in the same folder as Intel® FIT tool
2	**Generate Intermediate Files**	Yes	Yes/No - Yes is default
3	**Enable Boot Guard warning message at build time**	Yes	Yes/No - Yes is default
4	**Enable Intel(R) Platform Trust Technology warning message at build time**	Yes	Yes/No - Yes is default
5	**CPU Stepping**	Stepping B	Stepping A is default, Stepping B is alternate choice

Table 2-2. Intel® FIT - Build Settings (Sheet 2 of 2)

Click on Build Button in the top menu bar> Build Settings window pop up is displayed:			
#	Parameter	CRB	Values
6	**Region Order**		
7			$WorkingDir and $DestDir can be left at the default '.' Click on $SourceDir Value field and type in path where the Image Components are located for the Manageability Engine kit

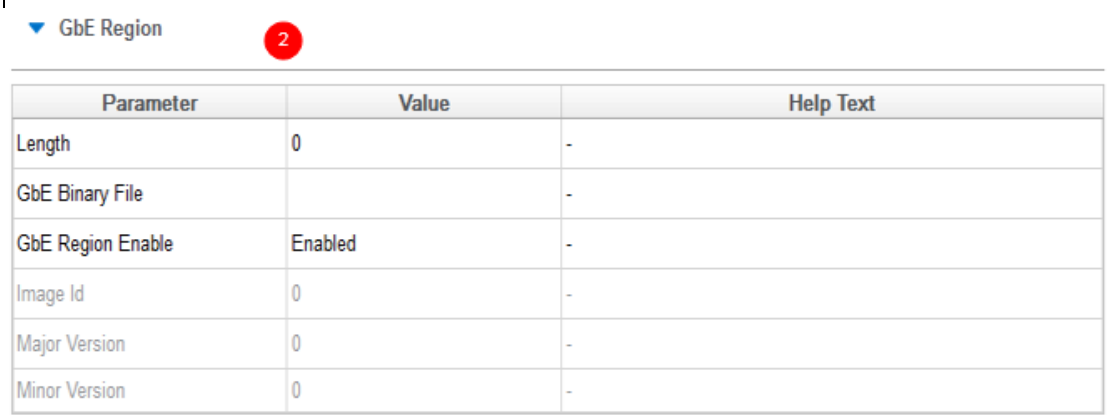
Table 2-3. Intel® FIT - Flash Layout (Sheet 1 of 5)

Click on Flash Layout in the left tabs menu> Descriptor Region is expanded by default:



#	Parameter	Platform	Settings
1	**Descriptor Region - Length** **Values: Leave this at zero.** Allows Intel® FIT to auto-size the descriptor region length.	SKL-Y SKL-U SKL-H SKL-S	0 0 0 0
	OEM Section Binary This loads the OEM Section binary that will be merged into the output image generated by the Intel® FIT tool.		

Click on Flash Layout in the left tabs menu> Gbe Region is expanded by default:



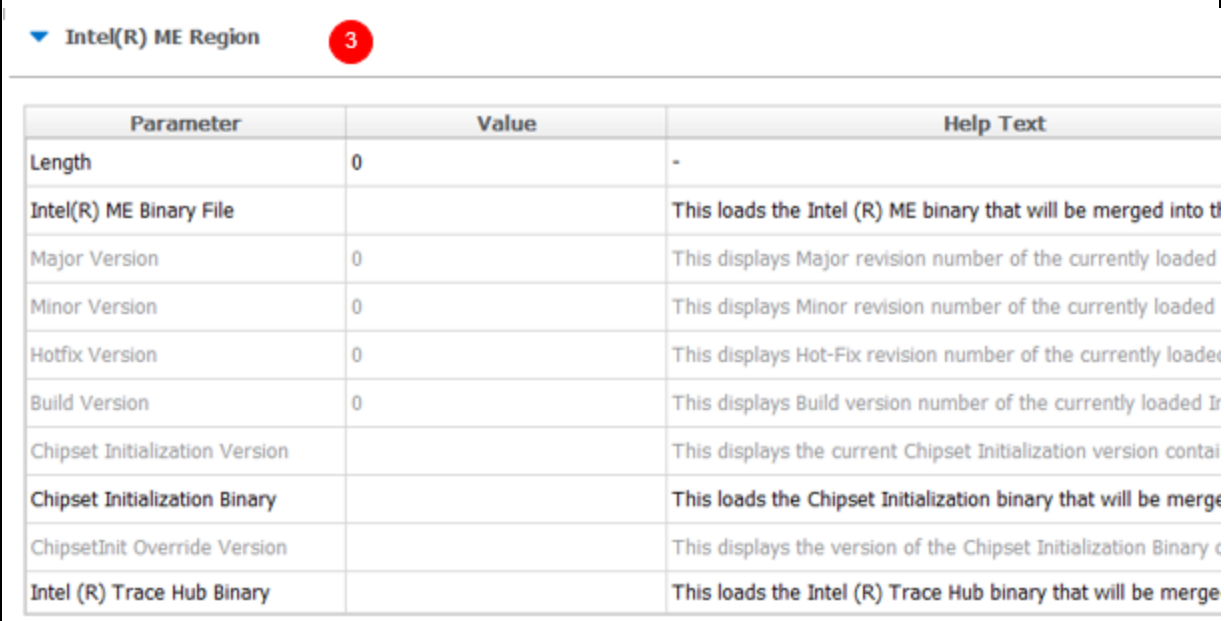
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Table 2-3. Intel® FIT - Flash Layout (Sheet 2 of 5)

<table>
<tr><th>#</th><th>Parameter</th><th>Platform</th><th>Settings</th></tr>
<tr><td>2</td><td>GbE Region - Length
Note: This value will be automatically populated by Intel® FIT during image build.</td><td>SKL-Y
SKL-U
SKL-H
SKL-S</td><td>0
0
0
0</td></tr>
<tr><td></td><td>GbE Binary File
Navigate to your Source Directory (as specified in Table 2-2) and switch to the GbE subdirectory. Choose the appropriate Intel GbE LAN Firmware binary image. If not using Intel LAN then load the GbE image before disabling the region along with changing additional settings below. This loads the Intel® integrated LAN binary that will be merged into the output image generated by the Intel® FIT tool.
Note: If loading gbeimage.bin file, check that the GbE region is enabled in tool before building image.</td><td>SKL-Y
SKL-U
SKL-H
SKL-S</td><td>gbeimage.bin
gbeimage.bin
gbeimage.bin
gbeimage.bin</td></tr>
<tr><td></td><td>GbE Region Enable
Values: Enabled / Disabled - This option allows the user to enable or disable the Gigabit Ethernet Region.
NOTE: If choosing a configuration that does not include the GbE LAN the following settings need to be adjusted:</td><td>SKL-Y
SKL-U
SKL-H
SKL-S</td><td>Enabled
Enabled
Enabled
Enabled</td></tr>
<tr><td colspan="4">
<table>
<tr><th>Name</th><th>Location</th><th>Value</th></tr>
<tr><td>LAN PHY Power Control GPD11 Signal Configuration</td><td>Offset 0x164 [7:6] LP
Offset 0x1A0 [7:6] H</td><td>00b</td></tr>
<tr><td>Gbe MAC SMBus Address Enable</td><td>Offset 0x147 [0] LP
Offset 0x183 [0] H</td><td>0b</td></tr>
<tr><td>PHY Connection</td><td>Offset 0x192 [2:0] LP
Offset 0x1CE [2:0] H</td><td>00b</td></tr>
<tr><td>Intel® PHY Over PCIe Enable</td><td>Offset 0x17C [6] LP
Offset 0x1B8 [6] H</td><td>0b</td></tr>
<tr><td>Intel® Integrated wired LAN Enable</td><td>Offset 0x1BC [6] LP
Offset 0x20C [6] H</td><td>0b</td></tr>
</table>
These additional settings are under the Networking & Connectivity tab > Wired LAN Configuration. In the GPIO > LAN / GPIO Select ensure the value is set correctly for board type.
</td></tr>
<tr><td></td><td>Image Id - This displays Image ID of the currently loaded Intel® Integrated LAN binary.</td><td></td><td></td></tr>
<tr><td></td><td>Major Version - This displays Major revision number of the currently loaded Intel® Integrated LAN binary.</td><td></td><td></td></tr>
<tr><td></td><td>Minor Version - This displays Minor revision number of the currently loaded Intel® Integrated LAN binary.</td><td></td><td></td></tr>
</table>

Table 2-3. Intel® FIT - Flash Layout (Sheet 3 of 5)

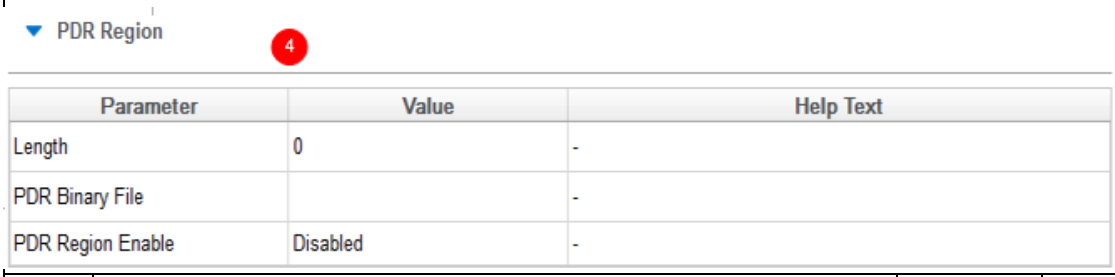
Click on Flash Layout in the left tabs menu> Intel® ME Region is expanded by default:



#	Parameter	Platform	Settings
3	**Intel® ME Region - Length**	SKL-Y SKL-U SKL-H SKL-S	0 0 0 0
	Intel® ME Binary File Navigate to your **Source Directory** (as specified in Table 2-2) and switch to the ME subdirectory. Choose the appropriate Intel **ME** Firmware binary image. This loads the Intel® ME binary that will be merged into the into the output image generated by the Intel® FIT tool. **Note:** You may choose to build the Intel® ME Region only. To do so, the **Number of Flash Components** in **Flash Settings> Flash Components** must be set to 0. **Note:** If loading meimage.bin file, check that the ME region is enabled in tool before building image.	SKL-Y SKL-U SKL-H SKL-S	meimage.bin meimage.bin meimage.bin meimage.bin
	Major Version - This displays Major revision number of the currently loaded Intel® ME binary.		
	Minor Version - This displays Minor revision number of the currently loaded Intel® ME binary.		
	Hotfix Version - This displays Hot-Fix revision number of the currently loaded Intel® ME binary.		
	Build Version - This displays Build version number of the currently loaded Intel® ME binary.		
	Chipset Initialization Binary - This loads the Chipset Initialization binary that will be merged into the output image generated by the Intel® FIT. If specified, this will override the version contained in the Intel® ME binary.		
	Chipset Initialization Version - This displays the current Chipset Initialization version contained in the currently loaded Intel® ME binary.		
	ChipsetInit Override Version - This displays the version of the Chipset Initialization Binary override if specified.		
	Intel® Trace Hub Binary - This loads the Intel® Trace Hub binary that will be merged into the output image generated by the Intel® FIT tool.		

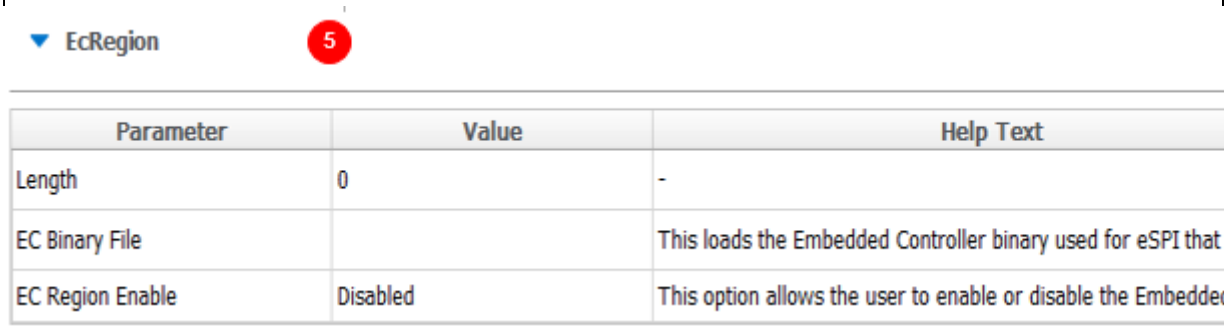
Table 2-3. Intel® FIT - Flash Layout (Sheet 4 of 5)

Click on Flash Layout in the left tabs menu> PDR Region is expanded by default:



#	Parameter	Platform	Settings
4	**PDR Region - Length** Region is disabled by default. Displays Region size information when **Binary input file** is specified.	SKL-Y SKL-U SKL-H SKL-S	0 0 0 0
	PDR Binary File Navigate to path to load pdrimage.bin file if required and available. This loads the Platform Data region binary that will be merged into the output image generated by the Intel® FIT tool.	SKL-Y SKL-U SKL-H SKL-S	- - - -
	PDR Region Enable **Values: Enabled / Disabled -** This option allows the user to enable or disable the Platform Data Region. **Note:** If loading PDR.bin file, check that the PDR region is enabled in tool before building image.	SKL-Y SKL-U SKL-H SKL-S	Disabled Disabled Disabled Disabled

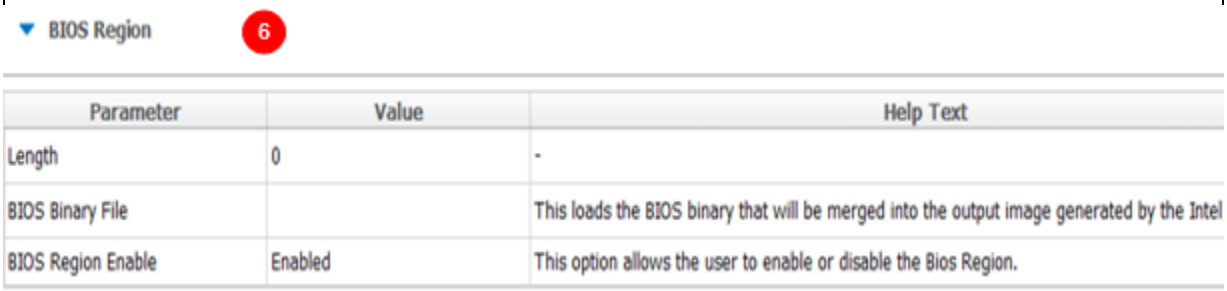
Click on Flash Layout in the left tabs menu> Ec Region is expanded by default:



#	Parameter	Platform	Settings
5	**EC Region - Length**	SKL-Y SKL-U SKL-H SKL-S	0 0 0 0
	EC Binary File Navigate to path to load EC bin file. This loads the Embedded Controller binary used for eSPI that will be merged into the output image generated by the Intel® FIT tool.	SKL-Y SKL-U SKL-H SKL-S	
	EC Region Enable **Values: Enabled / Disabled** This option allows the user to enable or disable the Embedded Controller data region.	SKL-Y SKL-U SKL-H SKL-S	Disabled Disabled Disabled Disabled

Table 2-3. Intel® FIT - Flash Layout (Sheet 5 of 5)

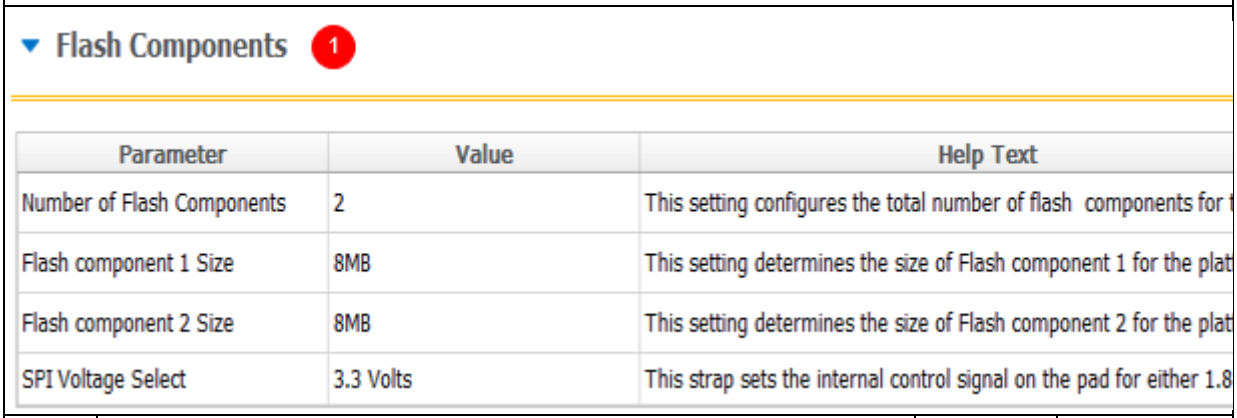
Click on Flash Layout in the left tabs menu> BIOS Region is expanded by default:



#	Parameter	Platform	Settings
6	**BIOS Region - Length**	SKL-Y SKL-U SKL-H SKL-S	0 0 0 0
	BIOS Binary File Navigate to path to load bios.rom file. This loads the BIOS binary that will be merged into the output image generated by the Intel® FIT tool.	SKL-Y SKL-U SKL-H SKL-S	
	BIOS Region Enable **Values: Enabled / Disabled** This option allows the user to enable or disable the BIOS region. **Note:** After loading bios.rom file, check that the BIOS region is enabled in tool before building image.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled

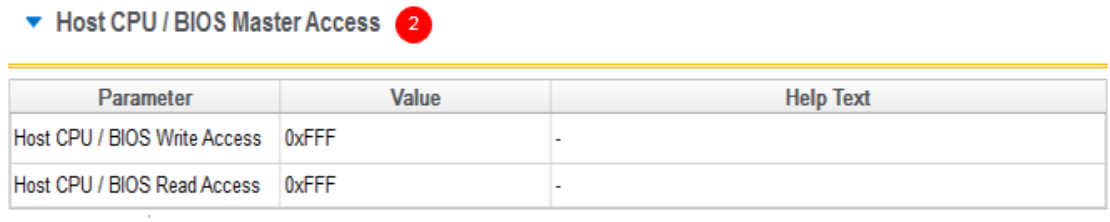
Table 2-4. Intel® FIT - Flash Settings (Sheet 1 of 7)

Click on Flash Settings in the left tabs menu> Flash Components is expanded by default:



#	Parameter	Platform	Settings
1	**Flash Components**		
	Number of Components **Values: 0, 1, 2 -** This setting configures the total number of flash components for the platform. **Note:** Choosing a selection of '0' part will cause the Intel® FIT tool to build an output image containing only the Intel® ME region.	SKL-Y SKL-U SKL-H SKL-S	1 1 1 1
	Flash component 1 Size **Values: 512KB, 1MB, 2MB, 4MB, 8MB, 16MB, 32MB, 64MB** - This setting determines the size of Flash component 1 for the platform image.	SKL-Y SKL-U SKL-H SKL-S	8MB 16MB 16MB 16MB
	Flash component 2 Size **Values: 512KB, 1MB, 2MB, 4MB, 8MB, 16MB, 32MB, 64MB** - This setting determines the size of Flash component 2 for the platform image. **Note:** This setting is only applicable when the Number of Flash Components option is set to '2'.	SKL-Y SKL-U SKL-H SKL-S	8MB 8MB 8MB 8MB
	SPI Voltage Select **Values: 1.8 Volts, 3.3 Volts** - This strap sets the internal control signal on the pad for either 1.8 or 3.3 volts. See Skylake H / LP SPI Programming Guide for further details.	SKL-Y SKL-U SKL-H SKL-S	3.3 Volts 3.3 Volts 3.3 Volts 3.3 Volts

Click on Flash Settings in the left tabs menu> Host CPU/BIOS Master Access is expanded by default:



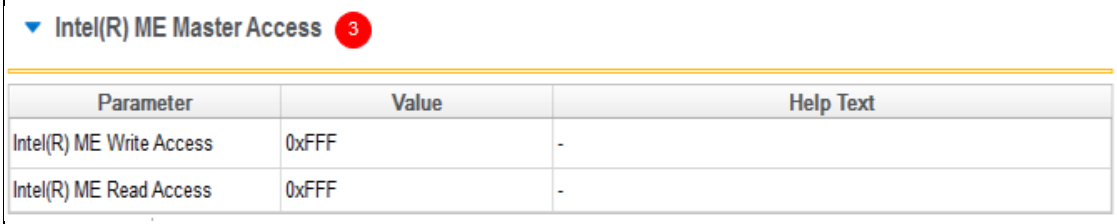
#	Parameter	Platform	Settings
2	**Host CPU / BIOS Master Access**		

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Table 2-4. Intel® FIT - Flash Settings (Sheet 2 of 7)

#	Parameter	Platform	Settings
	Host CPU / BIOS Write Access **Values: 0xFFF, 0x00A, 0x01A** - This setting determines write access control for the BIOS region. **0xFFF** = Debug/Manufacturing **0x00A** = Production **0x01A** = Production with access to PDR (should ONLY be used if PDR region is implemented). For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.	SKL-Y SKL-U SKL-H SKL-S	0xFFF 0xFFF 0xFFF 0xFFF
	Host CPU / BIOS Read Access **Values: 0xFFF, 0x00B, 0x01B** - This setting determines read access control for the BIOS region. **0xFFF** = Debug/Manufacturing **0x00B** = Production **0x01B** = Production with access to PDR (should ONLY be used if PDR region is implemented). For further details on Region Access Control see Skylake H / LP SPI Programming guide.	SKL-Y SKL-U SKL-H SKL-S	0xFFF 0xFFF 0xFFF 0xFFF

Click on Flash Settings in the left tabs menu> Intel® ME Master Access is expanded by default:



#	Parameter	Platform	Settings
3	**Intel® ME Master Access**		
	Intel® ME Write Access **Values: 0xFFF, 0x00C** - This setting determines write access control for the ME region. **0xFFF** = Debug/Manufacturing **0x00C** = Production For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.	SKL-Y SKL-U SKL-H SKL-S	0xFFF 0xFFF 0xFFF 0xFFF
	Intel® ME Read Access **Values: 0xFFF, 0x00D** - This setting determines read access control for the ME region. **0xFFF** = Debug/Manufacturing **0x00D** = Production For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.	SKL-Y SKL-U SKL-H SKL-S	0xFFF 0xFFF 0xFFF 0xFFF

Click on Flash Settings in the left tabs menu> GbE Master Access is expanded by default:

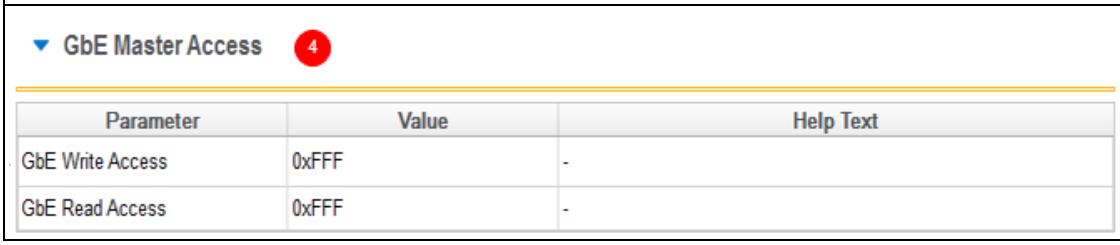
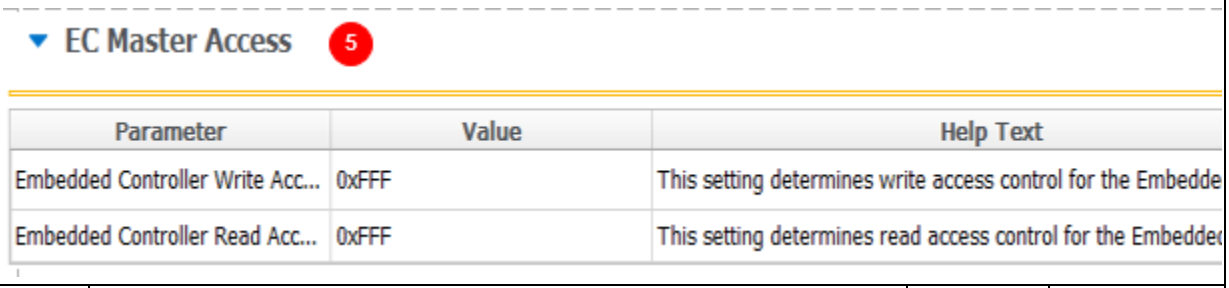


Table 2-4. Intel® FIT - Flash Settings (Sheet 3 of 7)

#	Parameter	Platform	Settings
4	**GbE Master Access**		
	GbE Write Access **Values: 0xFFF, 0x008** - This setting determines write access control for the Gigabit Ethernet Region. **0xFFF** = Debug/Manufacturing **0x008** = Production For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.	SKL-Y SKL-U SKL-H SKL-S	0xFFF 0xFFF 0xFFF 0xFFF
	GbE Read Access **Values: 0xFFF, 0x008** - This setting determines read access control for the Gigabit Ethernet Region. **0xFFF** = Debug/Manufacturing **0x008** = Production For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.	SKL-Y SKL-U SKL-H SKL-S	0xFFF 0xFFF 0xFFF 0xFFF

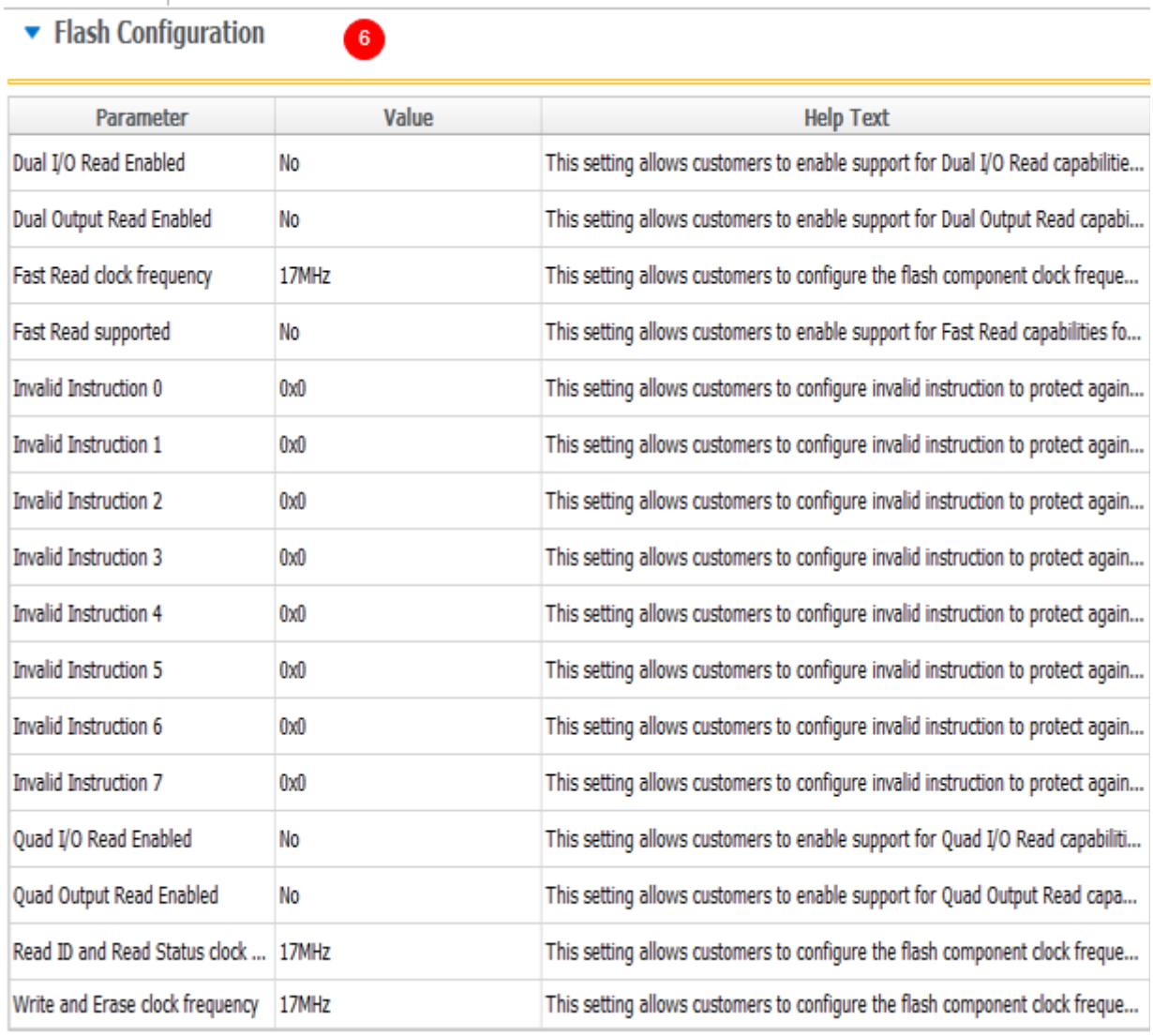
Click on Flash Settings in the left tabs menu> EC Master Access is expanded by default:



#	Parameter	Platform	Settings
5	**EC Master Access**		
#	**Parameter**	**Platform**	**Settings**
	EC Write Access **Values: 0xFFF, 0x020** - This setting determines write access control for the Embedded Controller Region. **0xFFF** = Debug/Manufacturing **0x020** = Production For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.	SKL-Y SKL-U SKL-H SKL-S	0xFFF 0xFFF 0xFFF 0xFFF
	EC Read Access **Values: 0xFFF, 0x008** - This setting determines read access control for the Embedded Controller Region. **0xFFF** = Debug/Manufacturing **0x020** = Production For further details on Region Access Control see Skylake H / LP SPI Programming guide further details.	SKL-Y SKL-U SKL-H SKL-S	0xFFF 0xFFF 0xFFF 0xFFF

Table 2-4. Intel® FIT - Flash Settings (Sheet 4 of 7)

Click on Flash Settings in the left tabs menu> Flash Configuration is expanded by default:



#	Parameter	Platform	Settings
6	**Flash Configuration**		
	Dual I/O Read Enabled **Values: Yes/No** - This setting allows the customer to enable support for Dual I/O Read capabilities for flash components. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Dual Output Read Enabled **Values: Yes/No** - This setting allows the customer to enable support for Dual Output Read capabilities for flash components. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	No No No Yes

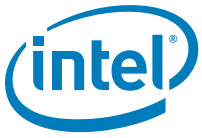
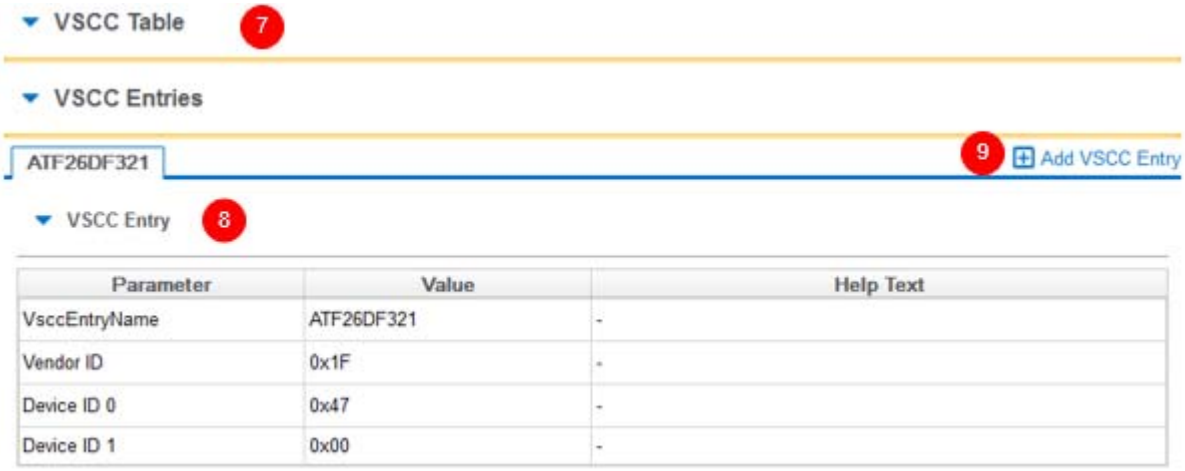


Table 2-4. Intel® FIT - Flash Settings (Sheet 5 of 7)

#	Parameter	Platform	Settings
	Fast Read Clock Frequency **Values: 17MHz, 30MHz, 48MHz** - This setting allows the customer to configure the flash component clock frequency setting for Fast Read. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	48MHz 48MHz 48MHz 48MHz
	Fast Read Supported **Values: Yes/No** - This setting allows the customer to enable support for Fast Read capabilities for flash components. See Skylake H / LP SPI Programming guide for further details. **Note:** If fast read supported is set to **"No"** any changes made to Dual I/O, Quad I/O, or Quad Output will not be affected if set to yes. Fast read supported should also be set to enable frequencies greater than 20MHz.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	Invalid Instruction 0 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. **Note:** This setting should be set to '0' if there are not Invalid instructions.	SKL-Y SKL-U SKL-H SKL-S	0x00000021 0x00000021 0x00000021 0x00000021
	Invalid Instruction 1 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. **Note:** This setting should be set to '0' if there are not Invalid instructions.	SKL-Y SKL-U SKL-H SKL-S	0x00000042 0x00000042 0x00000042 0x00000042
	Invalid Instruction 2 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. **Note:** This setting should be set to '0' if there are not Invalid instructions.	SKL-Y SKL-U SKL-H SKL-S	0x00000060 0x00000060 0x00000060 0x00000060
	Invalid Instruction 3 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. **Note:** This setting should be set to '0' if there are not Invalid instructions.	SKL-Y SKL-U SKL-H SKL-S	0x000000AD 0x000000AD 0x000000AD 0x000000AD
	Invalid Instruction 4 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. **Note:** This setting should be set to '0' if there are not Invalid instructions.	SKL-Y SKL-U SKL-H SKL-S	0x000000B7 0x000000B7 0x000000B7 0x000000B7
	Invalid Instruction 5 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. **Note:** This setting should be set to '0' if there are not Invalid instructions.	SKL-Y SKL-U SKL-H SKL-S	0x000000B9 0x000000B9 0x000000B9 0x000000B9
	Invalid Instruction 6 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. **Note:** This setting should be set to '0' if there are not Invalid instructions.	SKL-Y SKL-U SKL-H SKL-S	0x000000C4 0x000000C4 0x000000C4 0x000000C4
	Invalid Instruction 7 - This setting allows the customer to configure invalid instruction to protect against Chip Erase. See Skylake H / LP SPI Programming guide for further details. **Note:** This setting should be set to '0' if there are not Invalid instructions.	SKL-Y SKL-U SKL-H SKL-S	0x000000C7 0x000000C7 0x000000C7 0x000000C7
	Quad I/O Read Enabled **Values: Yes/No** - This setting allows the customer to enable support for Quad I/O Read capabilities for flash components. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Quad Output Read Enabled **Values: Yes/No** - This setting allows the customer to enable support for Quad Output Read capabilities for flash components. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	Read ID and Read Status clock frequency **Values: 17MHz, 30MHz, 48MHz** - This setting allows the customer to configure the flash component clock frequency setting for Read ID and Read Status. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	17MHz 17MHz 17MHz 17MHz

Table 2-4. Intel® FIT - Flash Settings (Sheet 6 of 7)

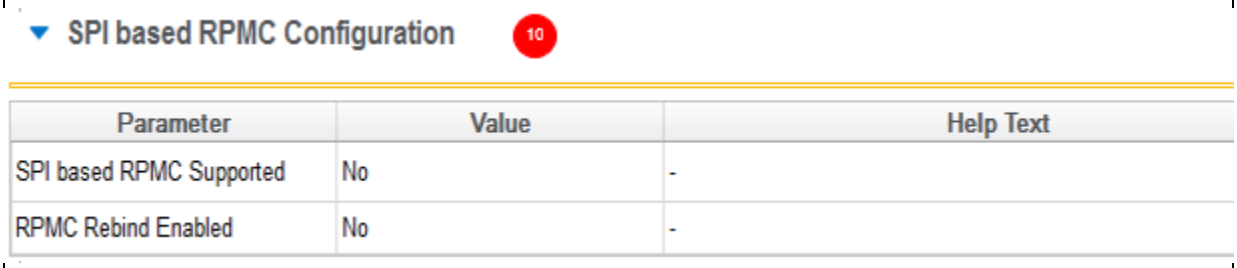
#	Parameter	Platform	Settings
	Write and Erase clock frequency **Values: 17MHz, 30MHz, 48MHz** - This setting allows the customer to configure the flash component clock frequency setting for Write and Erase. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	48MHz 48MHz 48MHz 48MHz
Click on Flash Settings in the left tabs menu> VSCC Table is expanded by default:			



#	Parameter	Platform	Settings
7	**Flash Settings - VSCC Table** **VSCC Entries**		
	ATF26DF321		
8	**VSCC Entry**		
	Name - This setting allow the OEM input a name designation for each flash component being used. **Note:** This is a free form entry field it does not affect actual flash component operation.	SKL-Y SKL-U SKL-H SKL-S	Winbond Winbond Winbond Winbond
	Vendor ID - This configures the JEDEC vendor specific byte ID of the SPI flash component. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	0xEF 0xEF 0xEF 0xEF
	Device ID 0 - This configures the JEDEC device specific byte ID 0 of the SPI flash component. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	0x40 0x40 0x40 0x40
	Device ID 1 - This configures the JEDEC device specific byte ID 1 of the SPI flash component. See Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	0x18 0x18 0x18 0x18
9	**+ Add VSCC Entry**		

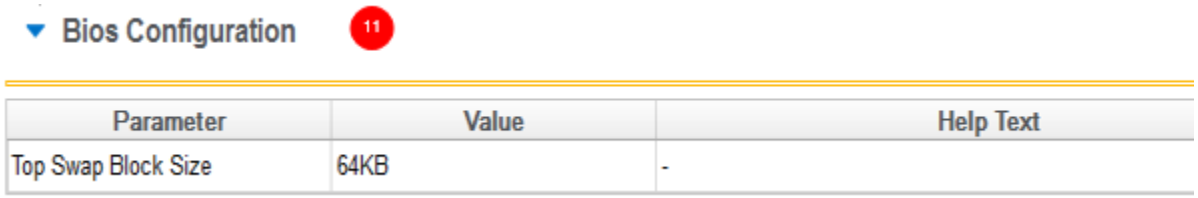
Table 2-4. Intel® FIT - Flash Settings (Sheet 7 of 7)

Click on Flash Settings in the left tabs menu> SPI based RPMC Configuration is expanded by default:



#	Parameter	Platform	Settings
10	**SPI based RPMC Configuration**		
	SPI based RPMC Supported **Values: Yes / No** - This setting configures SPI based Replay Protected Monotonic Counter support. **Note:** This setting only has effect when SPI part(s) supporting this feature are used. Consult SPI vendor data sheets to determine support for this feature.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	RPMC Rebind Enabled **Values: Yes / No -** This setting determines if RPMC rebinding is allowed. **Note:** This setting only has effect when the SPI part(s) support this feature are used.	SKL-Y SKL-U SKL-H SKL-S	No No No No

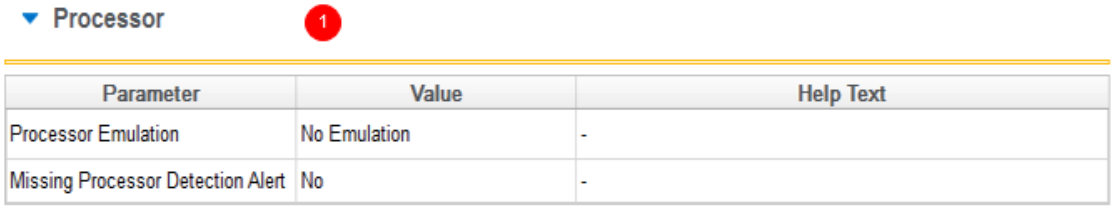
Click on Flash Settings in the left tabs menu> BIOS Configuration is expanded by default:



#	Parameter	Platform	Settings
11	**BIOS Configuration** **Top Swap Block Size** **Values: 64KB, 128KB, 256KB, 512KB, 1MB** - This configures the Top Swap Block size for the platform. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	64KB 64KB 64KB 64KB

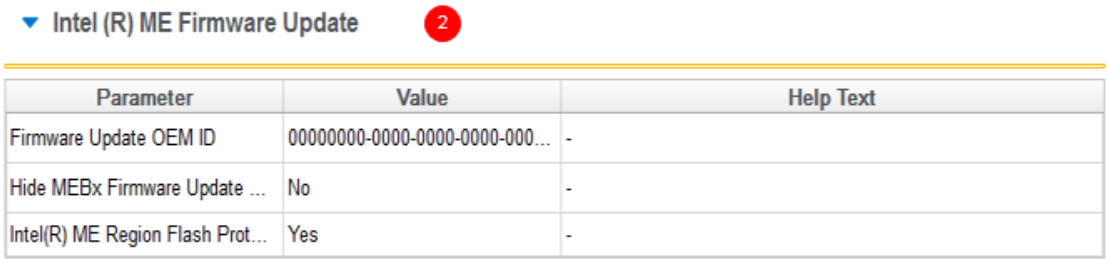
Table 2-5. Intel® FIT - Intel® ME Kernel (Sheet 1 of 5)

Click on Intel® ME Kernel in the left tabs menu> Processor is expanded by default:



#	Parameter	Platform	Settings
1	**Intel® ME Kernel - Processor**		
	Processor Emulation **Values: No Emulation** **EMULATE Intel® vPro (TM) capable Processor** **EMULATE Intel® Core (TM) branded Processor** **EMULATE Intel® Celeron (R) branded Processor** **EMULATE Intel® Pentium (R) branded Processor** **EMULATE Intel® Xeon (R) branded Processor** **EMULATE Intel® Xeon (R) Manageability capable Processor** This setting determines processor type to be emulated on pre-production silicon. Set this parameter to the type of processor that the target system will use during production. This field will emulate that processor class for pre-production silicon. It is necessary to set this to Emulate Intel® vPro™ Processor in order to enable Intel® AMT.	SKL-Y SKL-U SKL-H SKL-S	No Emulation No Emulation EMULATE Intel® vPro (TM) capable Processor EMULATE Intel® vPro (TM) capable Processor
	Missing Processor Detection Alert **Values: Yes / No -** This setting determines if missing processor detection is enabled on Desktop / Workstation platforms. **Note:** This feature will only work if the platform has the appropriate glue logic present.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No

Click on Intel® ME Kernel in the left tabs menu> Intel® ME Firmware Update is expanded by default:



#	Parameter	Platform	Settings
2	**Intel® ME Kernel - Intel® ME Firmware Update**		
	Firmware Update OEM ID - This setting allows configuration of an OEM unique ID to ensure that customers can only update their platform with images from the OEM of the platform.	SKL-Y SKL-U SKL-H SKL-S	0 string 0 string 0 string 0 string
	Hide Intel® MEBx Firmware Update Control **Values: Yes / No** - This setting allows the customer to hide the Firmware Update option in the Intel® MEBx interface.	SKL-Y SKL-U SKL-H SKL-S	No No No No

Table 2-5. Intel® FIT - Intel® ME Kernel (Sheet 2 of 5)

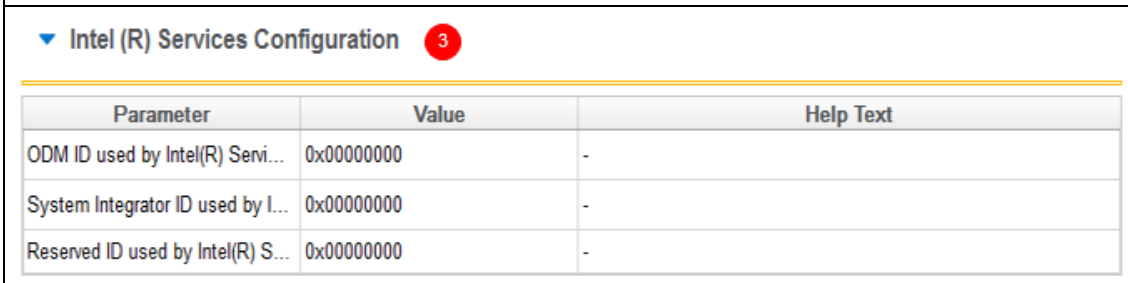
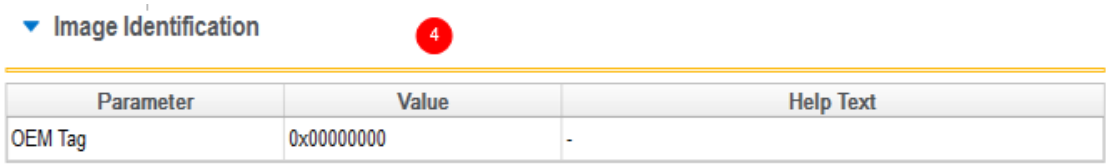
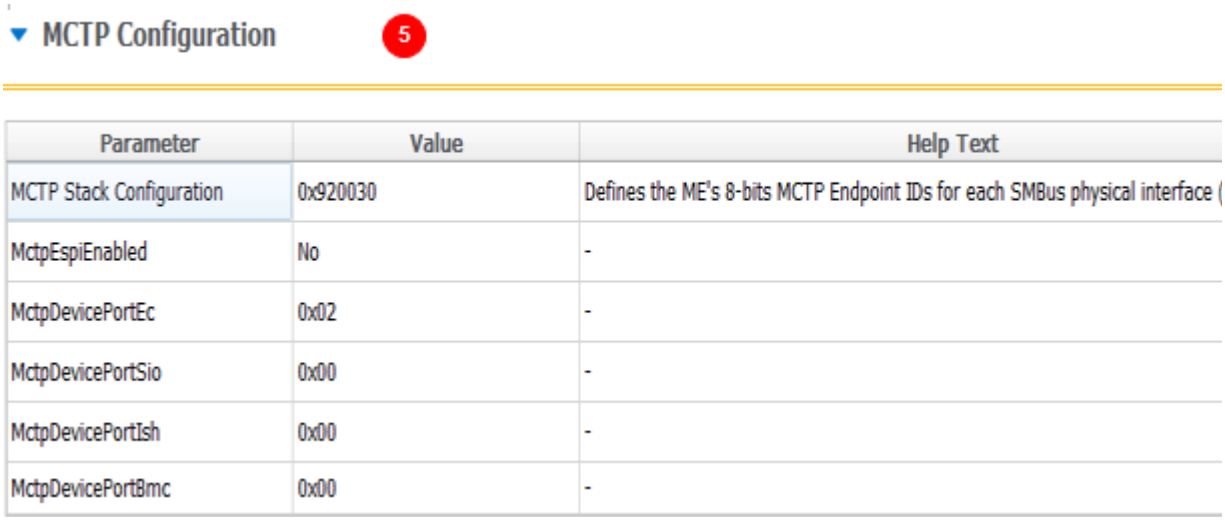
#	Parameter	Platform	Settings
	Intel® ME Region Flash Protection Override **Values: Yes/No** - This setting enables descriptor unlock of the Intel® ME Region when the HMRFPO message is sent to firmware prior to BIOS End of POST.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
Click on Intel® ME Kernel in the left tabs menu> Intel® ME Services Configuration is expanded by default:			
			
#	**Parameter**	**Platform**	**Settings**
3	**Intel® ME Kernel - Intel® Services Configuration**		
	ODM ID used by Intel® Services - This setting is for entering the ODM ID for Intel® Services to identify the ODM Board builder. **Note:** This ID is either generated by or registered with Intel® Services Web servers.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
	System Integrator ID used by Intel® Services - This setting is for entering the System Integrator ID for Intel® Services to identify the System Integrator. **Note:** This ID is either generated by or registered with Intel® Services Web servers.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
	Reserved ID used by Intel® Services - This setting is for entering the Reserved ID for Intel® Services currently not used.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
Click on Intel® ME Kernel in the left tabs menu> Image Identification is expanded by default:			
			
#	**Parameter**	**Platform**	**Settings**
4	**Intel® ME Kernel - Image Identification**		
	OEM Tag - This is a free form 32bit field that allows the OEM to configure their own unique identifier in the firmware image.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000

Table 2-5. Intel® FIT - Intel® ME Kernel (Sheet 3 of 5)

Click on Intel® ME Kernel in the left tabs menu> MCTP Configuration is expanded by default:

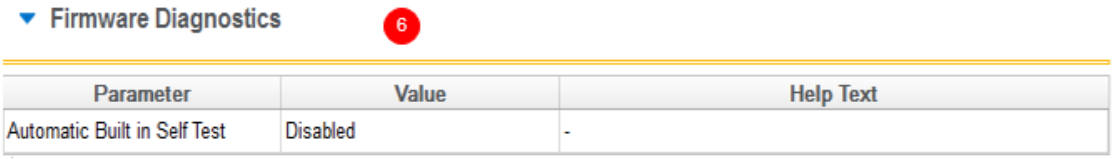


#	Parameter	Platform	Settings
5	**Intel® ME Kernel - MCTP Configuration**		
	MCTP Stack Configuration Defines the Intel® ME's 8-bits MCTP Endpoint ID's for each SMBus physical interface (SMBus, SMLink0, and SMLink1). These values are needed for FW to communicate with MCTP end points. For each of these 3 bytes, a value of 0x00 means not used, and values 0xFF or 0x01 - 0x07 or 0x20 - 0x2F are not allowed.	SKL-Y SKL-U SKL-H SKL-S	0x920030 0x920030 0x920030 0x920030
	MctpEspiEnabled **Value: Yes / No**	SKL-Y SKL-U SKL-H SKL-S	No No No No
	MctpDevicePortEc	SKL-Y SKL-U SKL-H SKL-S	0x0 0x0 0x0 0x0
	MctpDevicePortSio	SKL-Y SKL-U SKL-H SKL-S	0x00 0x00 0x00 0x00
	MctpDevicePortIsh	SKL-Y SKL-U SKL-H SKL-S	0x00 0x00 0x00 0x00
	MctpDevicePortBmc	SKL-Y SKL-U SKL-H SKL-S	0x00 0x00 0x00 0x00

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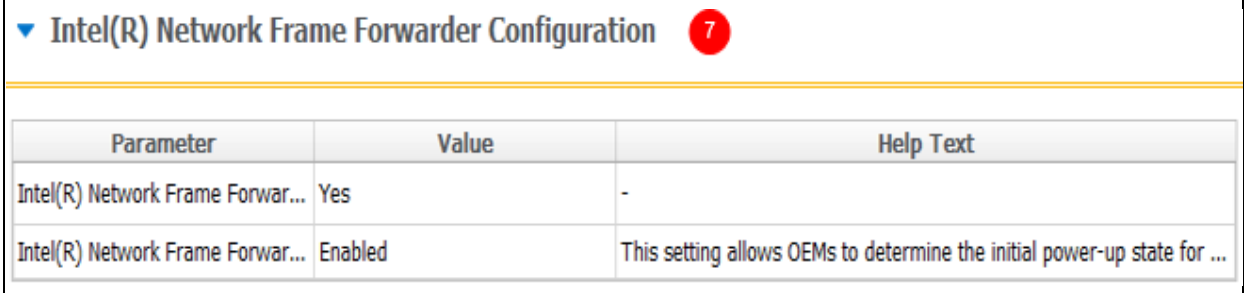
Table 2-5. Intel® FIT - Intel® ME Kernel (Sheet 4 of 5)

Click on Intel® ME Kernel in the left tabs menu> Firmware Diagnostics is expanded by default:



#	Parameter	Platform	Settings
6	**Intel® ME Kernel - Firmware Diagnostics**		
	Automatic Built in Self Test **Values: Enabled / Disabled** This setting enables the firmware Automatic Built in Self Test which is executed during first platform boot after initial image flashing.	SKL-Y SKL-U SKL-H SKL-S	Disabled Disabled Disabled Disabled

Click on Intel® ME Kernel in the left tabs menu> Intel® Network Frame Forwarder Configuration is expanded by default:



#	Parameter	Platform	Settings
7	**Intel® Network Frame Forwarder Configuration**		
	Intel® Network Frame Forwarder Supported **Values: Yes / No** **Note:** Some SPT-H may not support enabling of this option.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	Intel® Network Frame Forwarder Initial Power-Up State **Values: Enabled / Disabled** This setting allows OEMs to determine the initial power up state for Intel® Network Frame Forwarder feature.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled

Click on Intel® ME Kernel in the left tabs menu> Post Manufacturing Lock is expanded by default:

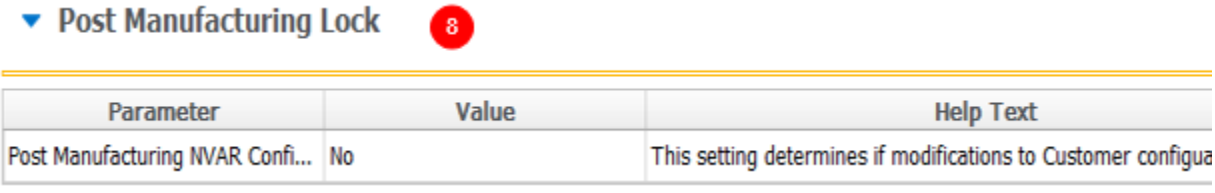


Table 2-5. Intel® FIT - Intel® ME Kernel (Sheet 5 of 5)

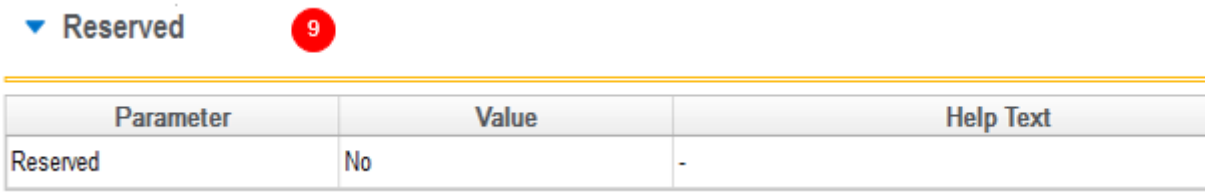
#	Parameter	Platform	Settings
8	**Intel® Post Manufacturing Lock**		
	Post Manufacturing NVAR Configuration Enabled **Values: Yes/No** This setting determines if modifications to Customer configurable NVARs is to be allowed after close of manufacturing.	SKL-Y SKL-U SKL-H SKL-S	No No No No
Click on Intel® ME Kernel in the left tabs menu> Reserved is expanded by default:			
			
#	Parameter	Platform	Settings
9	**Intel® ME Kernel - Reserved**		
	Reserved **Values: Yes/No**	SKL-Y SKL-U SKL-H SKL-S	No No No No

Table 2-6. Intel® FIT - Intel® AMT (Sheet 1 of 7)

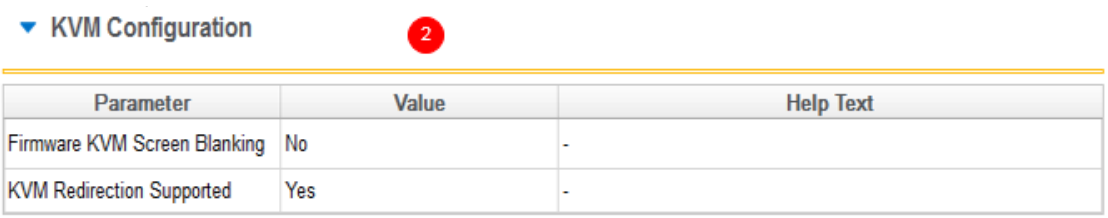
Click on Intel® AMT in the left tabs menu> Intel® AMT is expanded by default:



#	Parameter	Platform	Settings
1	**Intel® AMT - Intel® AMT Configuration**		
	Intel® AMT Supported **Values: Yes / No** - This setting allows customers to disable Intel® AMT on the platform and force the platform into Standard Manageability mode. **Note:** If this setting has been set to disabled Intel® AMT cannot be re-enabled once the descriptor has been locked. This setting applies to Desktop and Workstation only.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Intel® ME Network Services Supported **Values: Yes / No -** This setting allows customers to enable / disable Intel® ME Network Services on the platform. **Note:** If this setting is disabled Intel® AMT will also be disabled.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	Intel® Manageability Application Supported **Values: Yes / No -** This setting allows customers to force Intel® AMT enabled platforms to operate in Standard Manageability mode. **Note:** This setting only applies to Desktop and Workstation platforms.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Manageability Application initial power-up state **Values: Enabled / Disabled** This setting allows customers to determine the power up state for Intel® AMT or Standard Manageability. **Note:** If this setting is disabled Intel® AMT or Standard Manageability can still be re-enabled through the Intel® MEBx interface.	SKL-Y SKL-U SKL-H SKL-S	Disabled Disabled Disabled Disabled
	Intel® AMT Idle Timeout **Values: 0xFFFF** - This setting configures the idle timeout value before Intel® AMT enters into an off state.	SKL-Y SKL-U SKL-H SKL-S	0xFFFF 0xFFFF 0xFFFF 0xFFFF
	Intel® AMT Watchdog Automatic Reset Enabled **Values: Yes / No** - This setting allows customers to enable the Intel® ME firmware to trigger an automatic platform reset if either the MEI or Agent Presence are in a hung state. **Note:** This feature only allows one reset at a time when the watchdog expires. After this feature has triggered a reset, it must be re-armed for reuse via management console.	SKL-Y SKL-U SKL-H SKL-S	No No No No

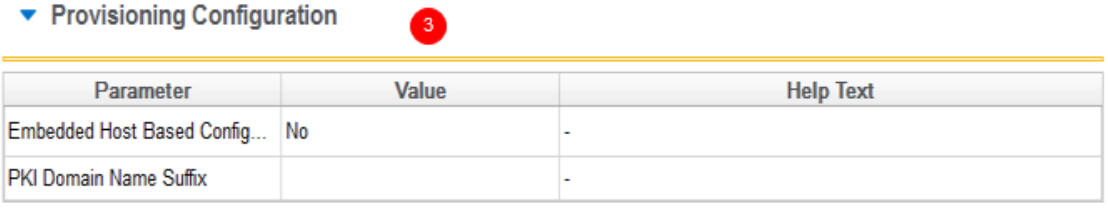
Table 2-6. Intel® FIT - Intel® AMT (Sheet 2 of 7)

Click on Intel® AMT in the left tabs menu> KVM Configuration is expanded by default:



#	Parameter	Platform	Settings
2	**Intel® AMT - KVM Configuration**		
	Firmware KVM Screen Blanking **Values: Yes/No -** This setting enables KVM Screen blanking capabilities in the firmware image. **Note:** This feature is dependent on processor level support.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	KVM Redirection Supported **Values: Yes/No** - This setting allows OEMs to enable / disable the KVM Redirection capabilities of the firmware. **Note:** If this setting has been set to disabled it cannot be re-enabled once the descriptor has been locked.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes

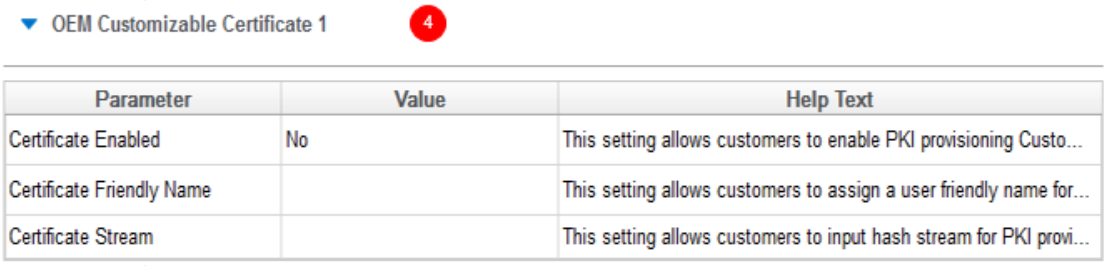
Click on Intel® AMT in the left tabs menu> Provisioning Configuration is expanded by default:



#	Parameter	Platform	Settings
3	**Intel® AMT - Provisioning Configuration**		
	Embedded Host Based Configuration **Values: Yes/No** - This setting allows customers to enable / disable Embedded Host Based Configuration. Important - EHBC is primarily intended for use in embedded systems as it offers less user privacy/security protection than may be appropriate for business client systems. **Note:** The Intel® FIT tool will not adjust the Redirection Privacy/Security value based on selection here. Please set security level as needed.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PKI Domain Name Suffix - This setting allow OEMs to pre-configure the Domain Name Suffix used for PKI provisioning in their firmware image. **Note:** For normal out-of-box provisioning functionality this setting should be left empty.		

Table 2-6. Intel® FIT - Intel® AMT (Sheet 3 of 7)

Click on Intel® AMT in the left tabs menu> OEM Customizable Certificate 1 is expanded by default:



#	Parameter	Platform	Settings
4	**Intel® AMT - OEM Customizable Certificate 1**		
	Certificate Enabled **Values: Yes/No** - This setting allows customers to enable PKI provisioning Custom Certificate 1.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friendly Name - This setting allows customers to assign a user friendly name for PKI provisioning Custom Certificate 1. Maximum of 32 characters.		
	Certificate Stream - This setting allows customers to input hash stream for PKI provisioning Custom Certificate 1. If enabled the certificate will be used in addition to those already pre-loaded in base firmware during provisioning. **Note:** If the platform is un-configured the Custom Certificate Hash will be deleted.		

Click on Intel® AMT in the left tabs menu> OEM Customizable Certificate 2 is expanded by default:



#	Parameter	Platform	Settings
5	**Intel® AMT - OEM Customizable Certificate 2**		
	Certificate Enabled **Values: Yes/No** - This setting allows customers to enable PKI provisioning Custom Certificate 2.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friendly Name - This setting allows customers to assign a user friendly name for PKI provisioning Custom Certificate 2. Maximum of 32 characters.		
	Certificate Stream - This setting allows customers to input hash stream for PKI provisioning Custom Certificate 2. If enabled the certificate will be used in addition to those already pre-loaded in base firmware during provisioning. **Note:** If the platform is un-configured the Custom Certificate Hash will be deleted.		

Table 2-6. Intel® FIT - Intel® AMT (Sheet 4 of 7)

Click on Intel® AMT in the left tabs menu> OEM Customizable Certificate 3 is expanded by default:



#	Parameter	Platform	Settings
6	**Intel® AMT - OEM Customizable Certificate 3**		
	Certificate Enabled **Values: Yes/No** - This setting allows customers to enable PKI provisioning Custom Certificate 3.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friendly Name - This setting allows customers to assign a user friendly name for PKI provisioning Custom Certificate 3. Maximum 32 characters.		
	Certificate Stream - This setting allows customers to input hash stream for PKI provisioning Custom Certificate 3. If enabled the certificate will be used in addition to those already pre-loaded in base firmware during provisioning. **Note:** If the platform is un-configured the Custom Certificate Hash will be deleted.		

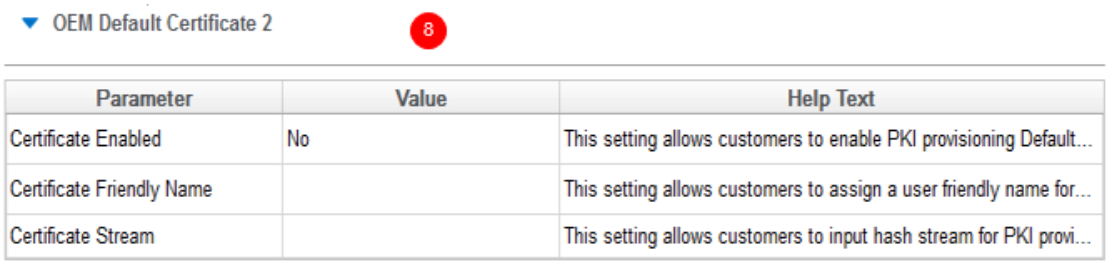
Click on Intel® AMT in the left tabs menu> OEM Default Certificate 1 is expanded by default:



#	Parameter	Platform	Settings
7	**Intel® AMT - OEM Default Certificate 1**		
	Certificate Enabled **Values: Yes/No** - This setting allows customers to enable PKI provisioning Default certificate 1.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friendly Name - This setting allows customers to assign a user friendly name for PKI provisioning Default Certificate 1. Maximum 32 characters.		
	Certificate Stream - This setting allows customers to input hash stream for PKI provisioning custom certificate 1. **Note:** Default Certificates if enabled will be used in addition to those already pre-loaded in firmware during provisioning. Unlike Customizable Certificates the Default Certificates are not deleted when the platform is un-provisioned.		

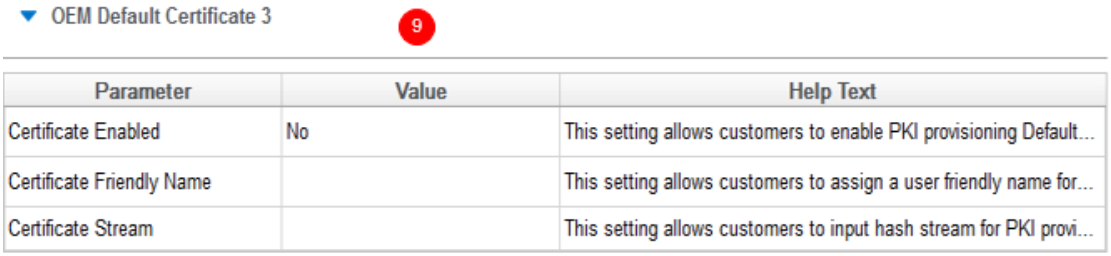
Table 2-6. Intel® FIT - Intel® AMT (Sheet 5 of 7)

Click on Intel® AMT in the left tabs menu> OEM Default Certificate 2 is expanded by default:



#	Parameter	Platform	Settings
8	**Intel® AMT - OEM Default Certificate 2**		
	Certificate Enabled **Values: Yes/No** - This setting allows customers to enable PKI provisioning Default certificate 2.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friendly Name - This setting allows customers to assign a user friendly name for PKI provisioning Default Certificate 2. Maximum 32 characters.		
	Certificate Stream - This setting allows customers to input hash stream for PKI provisioning custom certificate 2. **Note:** Default Certificates if enabled will be used in addition to those already pre-loaded in firmware during provisioning. Unlike Customizable Certificates the Default Certificates are not deleted when the platform is un-provisioned.		

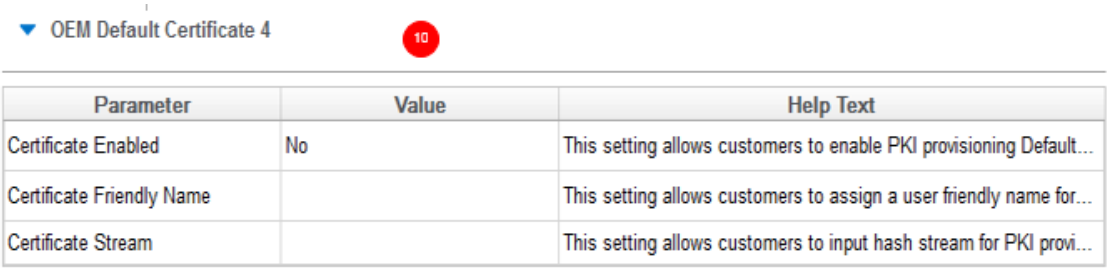
Click on Intel® AMT in the left tabs menu> OEM Default Certificate 3 is expanded by default:



#	Parameter	Platform	Settings
9	**Intel® AMT - OEM Default Certificate 3**		
	Certificate Enabled **Values: Yes/No** - This setting allows customers to enable PKI provisioning Default certificate 3.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friendly Name - This setting allows customers to assign a user friendly name for PKI provisioning Default Certificate 3. Maximum 32 characters.		
	Certificate Stream - This setting allows customers to input hash stream for PKI provisioning custom certificate 3. **Note:** Default Certificates if enabled will be used in addition to those already pre-loaded in firmware during provisioning. Unlike Customizable Certificates the Default Certificates are not deleted when the platform is un-provisioned.		

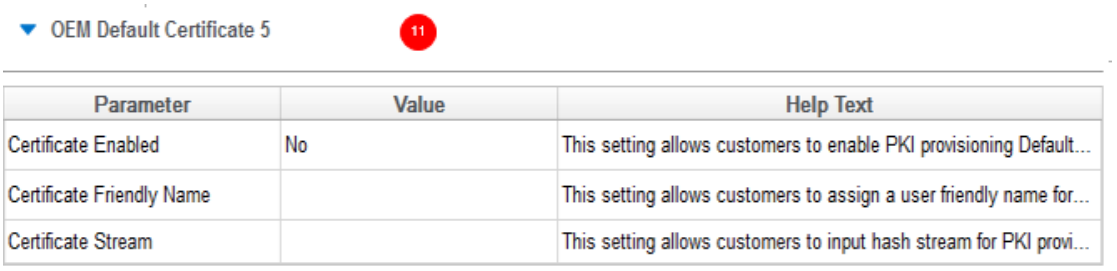
Table 2-6. Intel® FIT - Intel® AMT (Sheet 6 of 7)

Click on Intel® AMT in the left tabs menu> OEM Default Certificate 4 is expanded by default:



#	Parameter	Platform	Settings
10	**Intel® AMT - OEM Default Certificate 4**		
	Certificate Enabled **Values: Yes/No** - This setting allows customers to enable PKI provisioning Default certificate 4.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friendly Name - This setting allows customers to assign a user friendly name for PKI provisioning Default Certificate 4.		
	Certificate Stream - This setting allows customers to input hash stream for PKI provisioning custom certificate 4. **Note:** Default Certificates if enabled will be used in addition to those already pre-loaded in firmware during provisioning. Unlike Customizable Certificates the Default Certificates are not deleted when the platform is un-provisioned.		

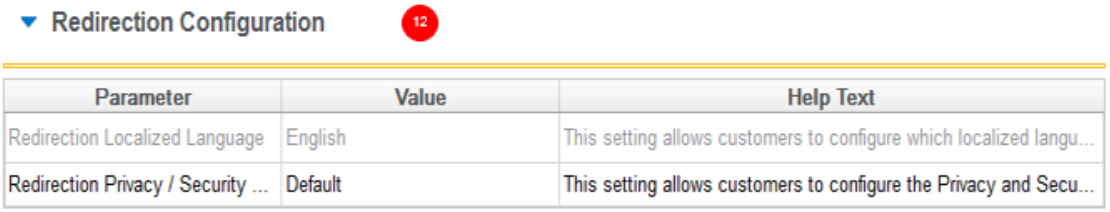
Click on Intel® AMT in the left tabs menu> OEM Default Certificate 5 is expanded by default:



#	Parameter	Platform	Settings
11	**Intel® AMT - OEM Default Certificate 5**		
	Certificate Enabled **Values: Yes/No** - This setting allows customers to enable PKI provisioning Default certificate 5.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Certificate Friendly Name - This setting allows customers to assign a user friendly name for PKI provisioning Default Certificate 5.		
	Certificate Stream - This setting allows customers to input hash stream for PKI provisioning custom certificate 5. **Note:** Default Certificates if enabled will be used in addition to those already pre-loaded in firmware during provisioning. Unlike Customizable Certificates the Default Certificates are not deleted when the platform is un-provisioned.		

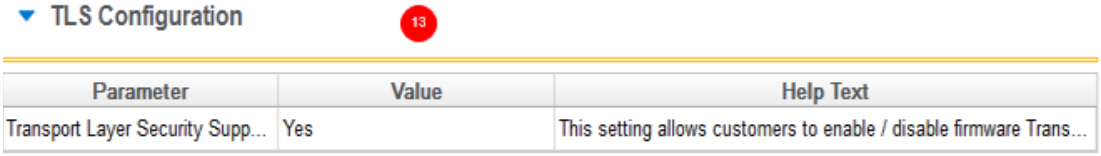
Table 2-6. Intel® FIT - Intel® AMT (Sheet 7 of 7)

Click on Intel® AMT in the left tabs menu> Redirection Configuration is expanded by default:



#	Parameter	Platform	Settings
12	**Intel® AMT - Redirection Configuration**		
	Redirection Localized Language - This setting allows customers to configure which localized language will be used initially by firmware for user consent output information (Examples: May be displayed before SOL / KVM session starts).	SKL-Y SKL-U SKL-H SKL-S	English English English English
	Redirection Privacy / Security Level - This setting allows customers to configure the Privacy and Security level for redirection operations. **Default** enables all redirection ports (User consent is configurable). **Enhanced** - Enables all redirection ports. (User consent is required and cannot be disabled). **Extreme -** Disables Redirection and Remote Configuration / Client Control Mode. **Note:** The Intel® FIT tool will not adjust the Embedded Host Based Configuration value based on selection here. Please set EHBC to yes or no as needed.	SKL-Y SKL-U SKL-H SKL-S	Default Default Default Default

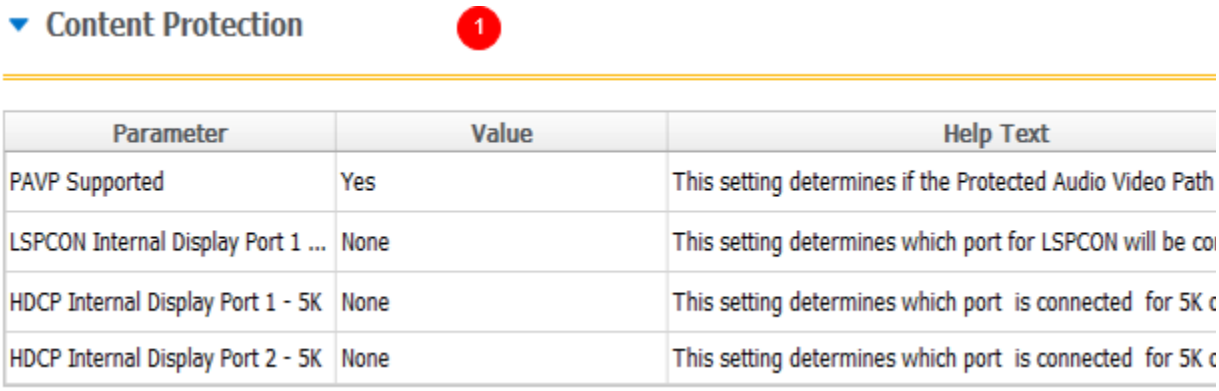
Click on Intel® AMT in the left tabs menu> TLS Configuration is expanded by default:



#	Parameter	Platform	Settings
13	**Intel® AMT - TLS Configuration**		
	Transport Layer Security Supported **Values: Yes/No** - This setting allows customers to enable / disable firmware Transport Layer Security support. **Note:** If this is disabled TLS will be permanently disabled in the firmware image.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes

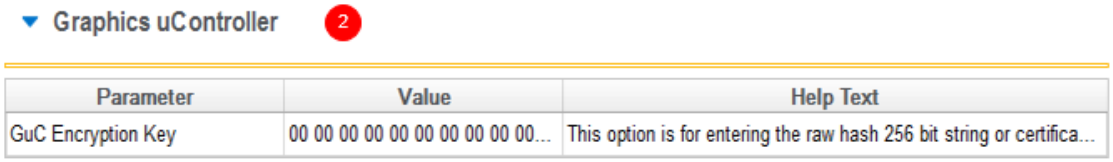
Table 2-7. Intel® FIT - Intel® Platform Protection (Sheet 1 of 4)

Click on Platform Protection in the left tabs menu> Content Protection is expanded by default:



#	Parameter	Platform	Settings
1	**Platform Protection - Content Protection**		
	PAVP Supported **Values: Yes / No** This setting determines if the Protected Audio Video Path (PAVP) feature will be permanently disabled in the FW image.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	LSPCON Internal Display Port 1 - LSPCON / 4K **Values: None, Port B, Port C, Port D** This setting determines which port for LSPCON will be connected to the HDCP 2.2 bridge adapter Display 1.	SKL-Y SKL-U SKL-H SKL-S	None None None None
	HDCP Internal Display Port 1 - 5K **Values: None, Port A, Port B, Port C, Port D** This setting determines which port is connected for 5K output on the Internal Display 1. **Note:** Both Display Port 1 & 2 need to be configured for proper operation.	SKL-Y SKL-U SKL-H SKL-S	None None None None
	HDCP Internal Display Port 2 - 5K **Values: None, Port A, Port B, Port C, Port D** This setting determines which port is connected for 5K output on the Internal Display 2. **Note:** Both Display Port 1 & 2 need to be configured for proper operation.	SKL-Y SKL-U SKL-H SKL-S	None None None None

Click on Platform Protection in the left tabs menu> Graphics uController is expanded by default:



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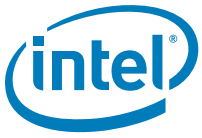
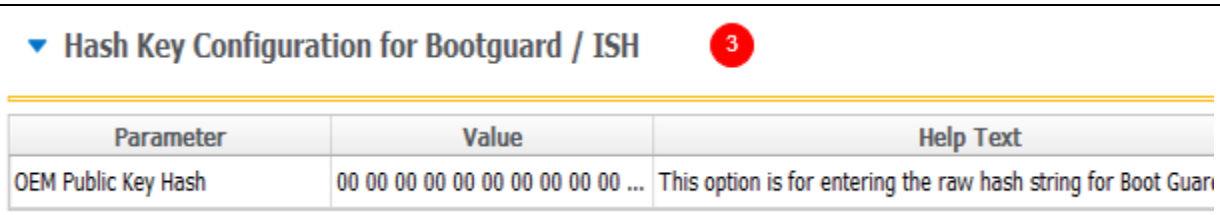


Table 2-7. Intel® FIT - Intel® Platform Protection (Sheet 2 of 4)

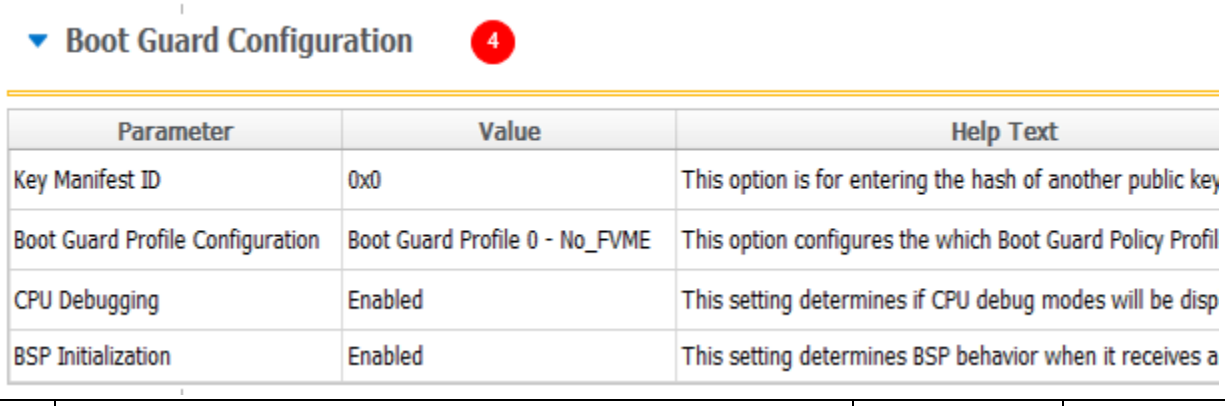
#	Parameter	Platform	Settings
2	**Platform Protection - Graphics UController**		
	GuC Encryption Key **Values:** This option is for entering the raw hash 256 bit string or certificate file for the Graphics uController.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000

Click on Platform Protection in the left tabs menu> Hash Key Configuration for Bootguard / ISH is expanded by default:



#	Parameter	Platform	Settings
3	**Platform Protection - Hash Key Configuration for Bootguard / ISH**		
	OEM Public Key Hash **Values:** This option is for entering the raw hash string or certificate file for Boot Guard and ISH. This 256-bit field represents the SHA-256 hash of the OEM public key corresponding to the private key used to sign the BIOS-SM or ISH image. Please see Appendix F for further details.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000

Click on Platform Protection in the left tabs menu> Boot Guard Configuration is expanded by default:

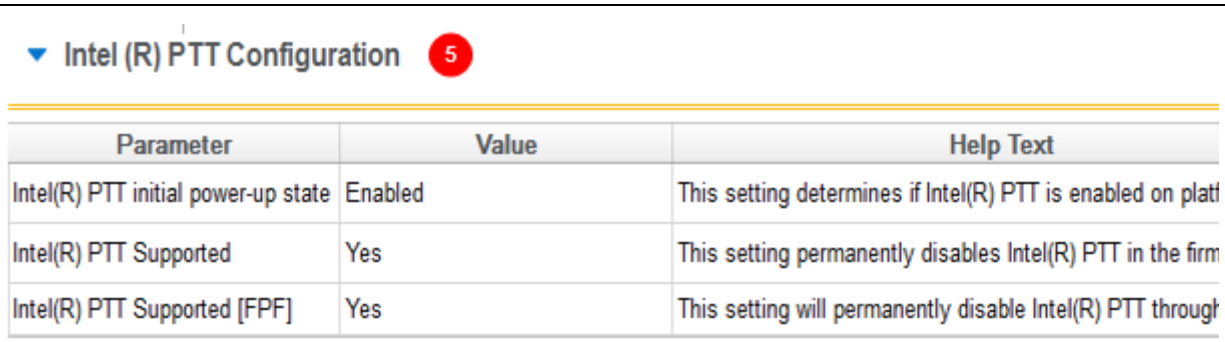


#	Parameter	Platform	Settings
4	**Platform Protection - Boot Guard Configuration**		
	Key Manifest ID **Values:** This option is for entering the hash of another public key, used by the ACM to verify the Boot Policy Manifest.	SKL-Y SKL-U SKL-H SKL-S	0x0 0x0 0x0 0x0

Table 2-7. Intel® FIT - Intel® Platform Protection (Sheet 3 of 4)

#	Parameter	Platform	Settings
	Boot Guard Profile Configuration **Values: Boot Guard Profile 0 - No_FVME** **Boot Guard Profile 1 - VE** **Boot Guard Profile 2 - VME** **Boot Guard Profile 3 - VM** **Boot Guard Profile 4 - FVE** **Boot Guard Profile 5 - FVME** This option configures which Boot Guard Policy Profile will be used.	SKL-Y SKL-U SKL-H SKL-S	Boot Guard Profile 0 - No_FVME Boot Guard Profile 0 - No_FVME Boot Guard Profile 0 - No_FVME Boot Guard Profile 0 - No_FVME
	CPU Debugging **Values: Enabled / Disabled** This setting determines if CPU debug modes will be displayed. When set to 'Enabled' CPU debugging is enabled.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	BSP Initialization **Values: Enabled / Disabled** This setting determines BSP behavior when it receives an INIT signal. When set to 'Enabled' BSP will behave normally if it receives an INIT (Disabled BSP Initialization (DBI) bit=0). When set to 'Disabled' BSP will shutdown if it receives an INIT ("DBI" bit=1).	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled

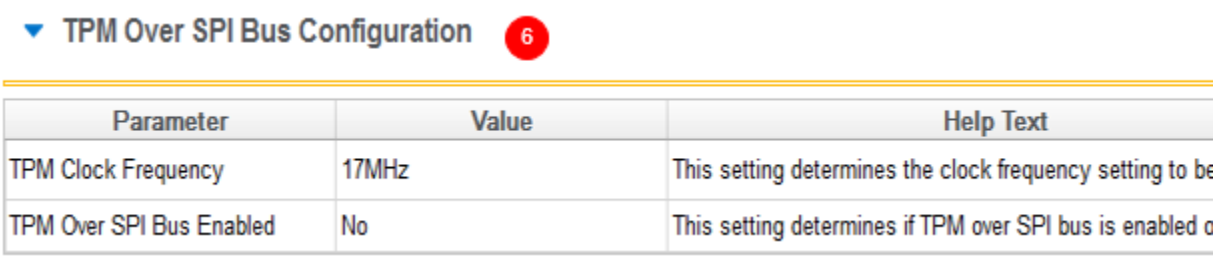
Click on Platform Protection in the left tabs menu> Intel® PTT Configuration is expanded by default:



#	Parameter	Platform	Settings
5	**Platform Protection - Intel® PTT Configuration**		
	Intel® PTT initial power-up state **Values: Enabled / Disabled** - This setting determines if Intel® PTT is enabled on platform power-up.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Disabled
	Intel® PTT Supported **Values: Yes / No** - This setting permanently disables Intel® PTT in the firmware image.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	Intel® PTT Supported [FPF] **Values: Yes / No** - This setting will permanently disable Intel® PTT through platform FPFs. **Caution:** Using this option will permanently disable Intel® PTT on the platform hardware.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes

Table 2-7. Intel® FIT - Intel® Platform Protection (Sheet 4 of 4)

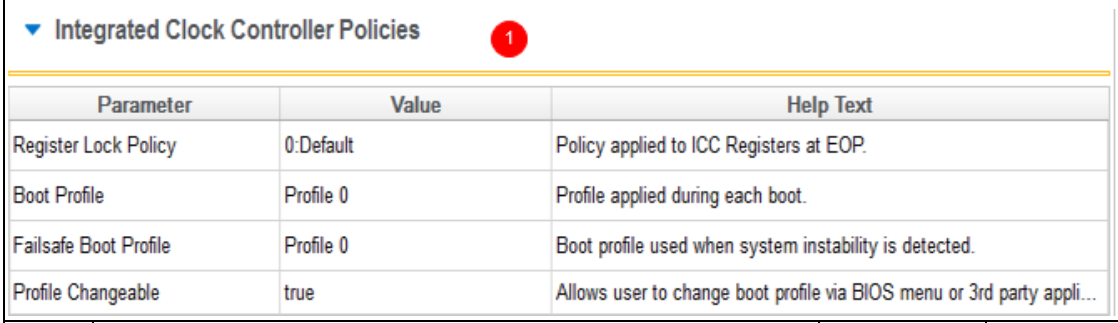
Click on Platform Protection in the left tabs menu> TPM Over SPI Bus Configuration is expanded by default:



#	Parameter	Platform	Settings
6	**Platform Protection - TPM Over SPI Bus Configuration**		
	TPM Clock Frequency **Values: 17MHz, 30MHz, 48MHz** - This setting determines the clock frequency setting to be used for the TPM over SPI bus.	SKL-Y SKL-U SKL-H SKL-S	17MHz 17MHz 17MHz 17MHz
	TPM Over SPI Bus Enabled **Values: Yes / No** - This setting determines if TPM over SPI bus is enabled on the platform.	SKL-Y SKL-U SKL-H SKL-S	No No No No

Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 1 of 13)

Click on Integrated Clock Controller in the left tabs menu> Integrated Clock Controller Policies are expanded by default:



#	Parameter	Platform	Settings
1	**Integrated Clock Controller - Integrated Clock Controller Policies**		
	Register Lock Policy **Values: 0:Default, 1:All Locked, 2: All Unlocked** This parameter controls Register lock policy. It defines the integrated clock registers left accessible to host after EOP. **0:Default** - Locks all but the registers associated to adjust BCLK nominal clock frequency and spread settings. **1:All Locked** - Locks all integrated clock registers and disables all writes to these registers via Intel® ME Firmware. **2:All Unlocked** - Leaves pre-EOP integrated clock registers unlocked.**This option is mainly used for debug purpose.** Double click on value column of this parameter to choose from available options.	SKL-Y SKL-U SKL-H SKL-S	0: Default 0: Default 0: Default 0: Default
	Boot Profile This parameter allows user to select default profile to be used by the final generated SPI Flash binary image for the target platform at boot time. Selection is limited to the profiles defined under “Integrated Clock Controller | Profiles “up to maximum 16 profiles. Profiles can be added by clicking on “Add profile” button under “Integrated Clock Controller | Profiles”. The ‘Record #’ refers to profile created under the “Integrated Clock Controller | Profiles”. Default boot profile for system is Profile 0. Double click on value column of this parameter to choose from available options.	SKL-Y SKL-U SKL-H SKL-S	Profile 0 Profile 0 Profile 0 Profile 0

Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 2 of 13)

#	Parameter	Platform	Settings
	Failsafe Profile This parameter specifies the profile index of the fail-safe profile. On boot failure detection or CMOS clear the Intel® ME Firmware will revert to this profile if "**Integrated Clock Controller |Integrated Clock Controller Policies - Profile Changeable "** is set to True. If profile Changeable parameter is set to False, User can not select Failsafe Boot Profile and profile 0 will be selected as a fail safe boot profile by default. The 'Record #' refers to profile created under the "Integrated Clock Controller | Profiles". Default Failsafe boot profile for system is Profile 0. Double click on value column of this parameter to choose from available options.	SKL-Y SKL-U SKL-H SKL-S	Profile 0 Profile 0 Profile 0 Profile 0
	Profile Changeable Possible configuration: True/False. This parameter controls if BIOS or 3rd party application can select boot profile or not. When set to true, it allows user to change boot profile via BIOS or 3rd party application. When set to false, Runtime change to boot profile is not allowed and boot profile selected by **"Integrated Clock Controller |Integrated Clock Controller Policies - Boot Profile "** parameter will be used to boot platform. Double click on value column of this parameter to choose from available options.	SKL-Y SKL-U SKL-H SKL-S	true true true true
Click on Integrated Clock Controller in the left tabs menu> Profiles are expanded by default:			

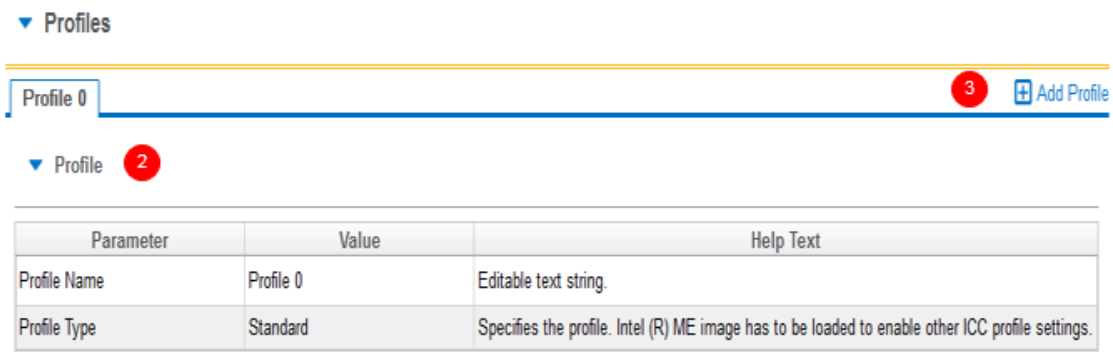
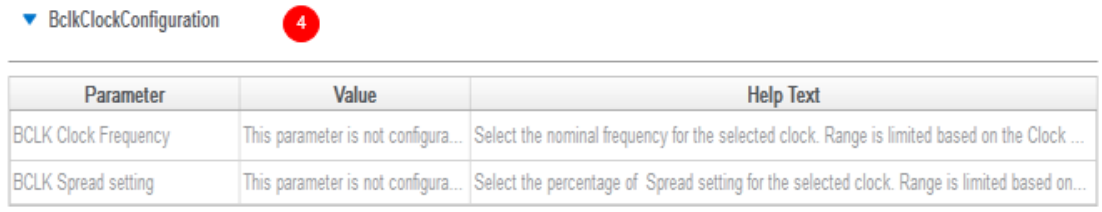


Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 3 of 13)

#	Parameter	Platform	Settings
2	**Integrated Clock Controller - Profiles - Profile 0** **For SKL-LP,** Intel® FIT provides 2 pre- defined ICC profiles to choose from. •**Standard**: This profile provides default settings for standard configuration, no adaptive clocking is allowed. Platform clocks output internal and external are driven from USB3PCIE clock. Default clock frequency is 100 MHz with 0.5%DownSpread. BCLK clock source should be turned off in this case to save power. •**Adaptive**: This profile provides Wimax/3G friendly configuration. This profile will configure the platform based on the Adaptive profile allowing adaptive clocking adjustment to reduce EMI interference. **Note:** Intel® ME image has to be loaded to enable other ICC profile settings. **For SKL-H,** Intel® FIT provides 4 pre-defined ICC profiles to choose from. •**Standard**: Same as SKL-LP •**Adaptive:** Same as SKL-LP •**Overclocking:** This profile provides overclocking friendly configuration. Both Clock sources BCLK and USB3PCIE are turned on in this case. clock frequency for BCLK and USB3PCIE clock is 100 MHz with 0.5%DownSpread. BCLK overclocking can be supported using BCLK clock source. •**Overclocking Plus:** This profile provides overclocking > 100MHZ for BCLK overclocking. **Note**: User can select pre-defined profiles via **"Integrated Clock Controller | Profiles - Profile Type "** parameter User can add up to maximum 16 profiles.To add new profile, please use **"Integrated Clock Controller | Profiles - + Add Profile Button"**	SKL-Y SKL-U SKL-H SKL-S	Standard Standard Standard Standard
	Profile Name This parameter allows user to customize profile name for easy identification. By default it uses pre-defined profile name like Profile 0.	SKL-Y SKL-U SKL-H SKL-S	Profile 0 Profile 0 Profile 0 Profile 0
	Profile Type Available ICC profiles for SKL-LP are Standard and Adaptive. Available ICC profiles for SKL-H are Standard, Adaptive, OverClocking, OverClockingPlus. This parameter indicates which pre- defined profile selected for each profile#. Double click on value column of this parameter to choose from available options.	SKL-Y SKL-U SKL-H SKL-S	Standard Standard Standard Standard
3	**+ Add Profile Button** This button is used to add new ICC profile. User can add up to maximum 16 profiles. New profile will be added under **"Integrated Clock Controller | Profiles"** tab**.**		

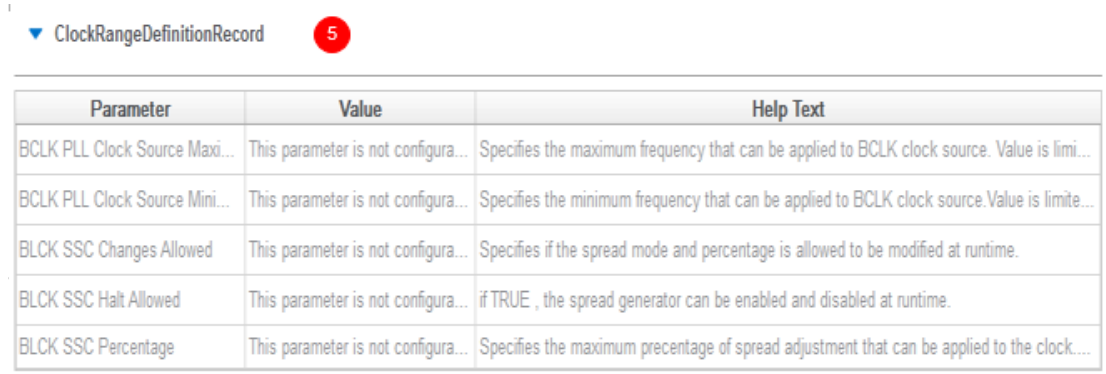
Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 4 of 13)

Click on Integrated Clock Controller in the left tabs menu> Profiles >Profile> Bclk Clock Configuration is expanded by default:



#	Parameter	Platform	Settings
4	**Integrated Clock Controller - Profiles - Profile BclkClockConfiguration**		
	BCLK Clock Frequency - This parameter allows user to select the nominal frequency for the selected clock. Range is limited based on the Clock Range Definition record and HW SKU. **Standard Setting Profile Type -** Option is grayed out. **Adaptive Setting Profile Type -** Option is able to be edited.		
	BCLK Spread Setting - This parameter allows user to select the percentage of Spread setting for the selected clock. Range is limited based on the Clock Range Definition record and HW SKU. **BCLK Clock Frequency** **Standard Setting Profile Type -** Option is grayed out. **Adaptive Setting Profile Type -** Option is able to be edited.		

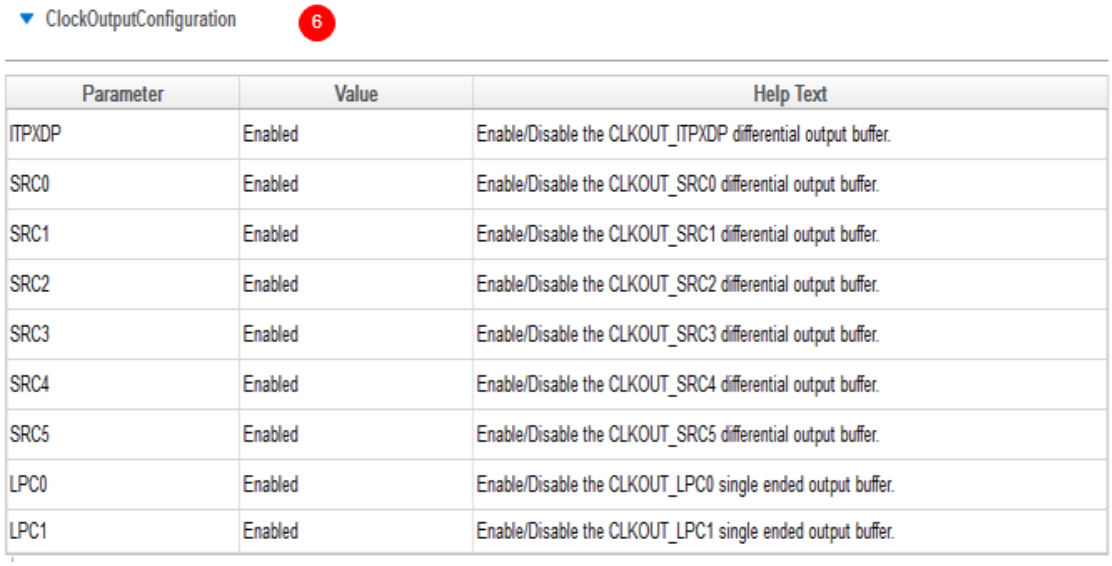
Click on Integrated Clock Controller in the left tabs menu> Profiles >Profile> Clock Range Definition Record is expanded by default:



#	Parameter	Platform	Settings
5	**Integrated Clock Controller - Profiles - Profile ClockRangeDefinitionRecord**		
	BCLK PLL Clock Source Maximum Frequency - This parameter allows user to specify the maximum frequency that can be applied to BCLK clock source. Value is limited by divider/frequency limits determined by HW SKU. **Standard Setting Profile Type -** Option is grayed out. **Adaptive Setting Profile Type -** Option is able to be edited.		

Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 5 of 13)

#	Parameter	Platform	Settings
	BCLK PLL Clock Source Minimum Frequency - This parameter allows user to specify the minimum frequency that can be applied to BCLK clock source. Value is limited by divider/frequency limits determined by HW SKU. **Standard Setting Profile Type -** Option is grayed out. **Adaptive Setting Profile Type -** Option is able to be edited.		
	BCLK SSC Changes Allowed - This parameter allows user to specify if the spread mode and percentage is allowed to be modified at runtime or not. if set to **"True':** Runtime modification is allowed. **Standard Setting Profile Type -** Option is grayed out. **Adaptive Setting Profile Type -** Option is able to be edited.		
	BCLK SSC Halt Allowed - This parameter allows user to select if the spread generator can be disabled at runtime or not.if set to **"True"**, the spread generator can be enabled and disabled at runtime. **Standard Setting Profile Type -** Option is grayed out. **Adaptive Setting Profile Type -** Option is able to be edited.		
	BCLK SSC Percentage - This parameter Specifies the maximum percentage of spread adjustment that can be applied to the clock. Value is specified in 1/100th of percent(50=0.5%) **Standard Setting Profile Type -** Option is grayed out. **Adaptive Setting Profile Type -** Option is able to be edited.		
Click on Integrated Clock Controller in the left tabs menu> Profiles >Profile> Clock Output Configuration is expanded by default:			



Parameter	Value	Help Text
ITPXDP	Enabled	Enable/Disable the CLKOUT_ITPXDP differential output buffer.
SRC0	Enabled	Enable/Disable the CLKOUT_SRC0 differential output buffer.
SRC1	Enabled	Enable/Disable the CLKOUT_SRC1 differential output buffer.
SRC2	Enabled	Enable/Disable the CLKOUT_SRC2 differential output buffer.
SRC3	Enabled	Enable/Disable the CLKOUT_SRC3 differential output buffer.
SRC4	Enabled	Enable/Disable the CLKOUT_SRC4 differential output buffer.
SRC5	Enabled	Enable/Disable the CLKOUT_SRC5 differential output buffer.
LPC0	Enabled	Enable/Disable the CLKOUT_LPC0 single ended output buffer.
LPC1	Enabled	Enable/Disable the CLKOUT_LPC1 single ended output buffer.

#	Parameter	Platform	Settings
6	**Integrated Clock Controller - Profiles - Profile Clock Output Configuration**		

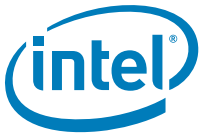


Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 6 of 13)

#	Parameter	Platform	Settings
	ITPXDP,SRC[0:5] **Values: Enabled / Disabled** These parameters come under the Power Management section and they control Enabling /Disabling of specific Output Clocks at boot time. These settings should match with platform hardware design. For CRB, recommend keeping defaults for bring up with Intel® ME FW. These parameters are specifically used to Enable/Disable the respective CLKOUT_XXX differential output buffers	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	SRC0[6:15] **Values: Enabled / Disabled** These parameters come under the Power Management section and they control Enabling /Disabling of specific Output Clocks at boot time. These settings should match with platform hardware design. For CRB, recommend keeping defaults for bring up with Intel® ME FW. These parameters are specifically used to Enable/Disable the respective CLKOUT_XXX differential output buffers	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	SRC1 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC1 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	SRC2 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC2 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	SRC3 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC3 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	SRC4 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC4 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	SRC5 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC5 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	SRC6 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC6 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	SRC7 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC7 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled

Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 7 of 13)

#	Parameter	Platform	Settings
	SRC8 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC8 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	SRC9 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC9 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	SRC10 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC10 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	SRC11 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC11 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	SRC12 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC12 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	SRC13 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC13 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	SRC14 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC14 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	SRC15 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_SRC15 differential output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	LPC0[1:0] **Values: Enabled / Disabled** These parameters are used to control Enabling/Disabling of CLKRUN support for CLKOUT_LPC clocks. For CRB, recommend keeping defaults for bring up with Intel® ME FW	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	LPC1 **Values: Enabled / Disabled** Enables or Disables the CLKOUT_LPC1 single ended output buffer.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	CPUPCIBCLK **Values: Enabled / Disabled** Enables or Disables the CPUPCIBCLK output buffer.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled

Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 8 of 13)

Click on Integrated Clock Controller in the left tabs menu> Profiles >Profile> Power Management Configuration is expanded by default:

▼ Power Management Configuration 7

Parameter	Value	Help Text
SRC0 CLKREQ# Mapping	GPP_B5	Assign the CLKREQ# signal associated with CLKOU
SRC1 CLKREQ# Mapping	GPP_B6	Assign the CLKREQ# signal associated with CLKOU
SRC2 CLKREQ# Mapping	GPP_B7	Assign the CLKREQ# signal associated with CLKOU
SRC3 CLKREQ# Mapping	GPP_B8	Assign the CLKREQ# signal associated with CLKOU
SRC4 CLKREQ# Mapping	GPP_B9	Assign the CLKREQ# signal associated with CLKOU
SRC5 CLKREQ# Mapping	GPP_B10	Assign the CLKREQ# signal associated with CLKOU
CLKREQ SRC0 Enable	Enabled	Enable/Disable the dynamic clock request control b
CLKREQ SRC1 Enable	Enabled	Enable/Disable the dynamic clock request control b
CLKREQ SRC2 Enable	Enabled	Enable/Disable the dynamic clock request control b
CLKREQ SRC3 Enable	Enabled	Enable/Disable the dynamic clock request control b
CLKREQ SRC4 Enable	Enabled	Enable/Disable the dynamic clock request control b
CLKREQ SRC5 Enable	Enabled	Enable/Disable the dynamic clock request control b
CLKRUN LPC0 Enable	Enabled	Enable/Disable the CLKRUN protocol on LPC0 outpu
CLKRUN LPC1 Enable	Enabled	Enable/Disable the CLKRUN protocol on LPC1 outpu
Clock Gating of Core 24Mhz Cry...	Enabled	Enable/Disable dynamic clock gating of Core 24Mh
Clock Gating of CLKOUT_ITPxD...	Enabled	Enable/Disable dynamic control of CLKOUT_ITPxDP
Clock Gating of CLKOUT_CPUBC...	Enabled	Enable/Disable dynamic control of CLKOUT_CPUBC
Clock Gating of CLKOUT_CPUNS...	Enabled	Enable/Disable dynamic control of CLKOUT_CPUNS
Clock Gating of CLKOUT_CPUNS...	Enabled	Enable/Disable dynamic control of CLKOUT_CPUNS
Clock Gating of icc_rosc_fast_cl...	Enabled	Enable/Disable dynamic clock gate on icc_rosc_fas
Clock Gating of icc_rosc_side_cl...	Enabled	Enable/Disable dynamic clock gate on icc_rosc_sid
USB3Gen2PCIe PLL OFF Wait	8us	Set G2PLLOFFWAIT timer value. Once timer exprir
USB3Gen2PCIe PLL PG Wait	8us	Set G2PLLPGWAIT timer value. Once timer exprire
Run-time S0 SUS PG Wait	8us	Set SUSPGWAIT timer value. Once timer exprires
Crystal Oscillator Fast Restart ...	01b	Configure Crystal Oscillator Fast Restart Mode. In
BCLK PLL Shutdown Wait Interval	8us	Enable Dynamic power management of BCLK PLL.
24Mhz Crystal Shutdown Wait I...	8us	Enable Dynamic power management of Crystal. Up

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Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 9 of 13)

#	Parameter	Platform	Settings
7	**Integrated Clock Controller - Profiles - Profile PwrManagementConfiguration**		
	SRC0[5:0] CLKREQ# Mapping Possible configuration: Select one of the GPIOs from the list to map it as a CLKREQ# for specific SRC# Output clock. This parameter controls association of dynamic CLKREQ control with SRC (PCIe) clocks. **SRC[15:6] CLKREQ# Mapping - SKL - H Only** Possible configuration: Select one of the GPIOs from the list to map it as a CLKREQ# for specific SRC# Output put clock. This parameter controls association of dynamic CLKREQ control with SRC (PCIe) clocks.	SKL-Y SKL-U SKL-H SKL-S	GPP_B5 GPP_B5 GPP_B5 GPP_B5
	SRC1 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC1.	SKL-Y SKL-U SKL-H SKL-S	GPP_B6 GPP_B6 GPP_B6 GPP_B6
	SRC2 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC2.	SKL-Y SKL-U SKL-H SKL-S	GPP_B7 GPP_B7 GPP_B7 GPP_B7
	SRC3 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC3.	SKL-Y SKL-U SKL-H SKL-S	GPP_B8 GPP_B8 GPP_B8 GPP_B8
	SRC4 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC4.	SKL-Y SKL-U SKL-H SKL-S	GPP_B9 GPP_B9 GPP_B9 GPP_B9
	SRC5 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC5.	SKL-Y SKL-U SKL-H SKL-S	GPP_B10 GPP_B10 GPP_B10 GPP_B10
	SRC6 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC6.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H0 GPP_H0
	SRC7 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC7.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H1 GPP_H1
	SRC8 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC8.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H2 GPP_H2
	SRC9 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC9.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H3 GPP_H3
	SRC10 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC10.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H4 GPP_H4

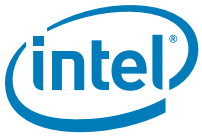


Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 10 of 13)

#	Parameter	Platform	Settings
	SRC11 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC11.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H5 GPP_H5
	SRC12 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC1.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H6 GPP_H6
	SRC13 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC13.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H7 GPP_H7
	SRC14 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC14.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H8 GPP_H8
	SRC15 CLKREQ# Mapping Assign the CLKREQ# signal associated with CLKOUT_SRC15.	SKL-Y SKL-U SKL-H SKL-S	NA NA GPP_H9 GPP_H9
	CLKREQ SRC0 [5:0] Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC[5:0] **CLKREQ SRC [15:6] enable - SKL-H Only** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC[15:6]	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	CLKREQ SRC1 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC1.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	CLKREQ SRC2 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC2.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	CLKREQ SRC3 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC3.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	CLKREQ SRC4 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC4.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	CLKREQ SRC5 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC5.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	CLKREQ SRC6 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC6.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKREQ SRC7 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC7.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled

Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 11 of 13)

#	Parameter	Platform	Settings
	CLKREQ SRC8 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC8.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKREQ SRC9 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC9.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKREQ SRC10 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC10.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKREQ SRC11 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC11.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKREQ SRC12 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC12.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKREQ SRC13 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC13.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKREQ SRC14 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC14.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKREQ SRC15 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable the dynamic clock request control by the assigned CLKREQ# for CLKOUT_SRC15.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	CLKRUN LPC0 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable CLKRUN protocol on LPC1 output clock.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	CLKRUN LPC1 Enable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable CLKRUN protocol on LPC1 output clock.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	Clock Gating of Core 24MHz Crystal Disable **Values: Enabled / Disabled** This parameter decides if Crystal is forced to be on or is subjected to dynamic shutdown. Crystal Oscillator can dynamically shut down upon iSCLK detecting idle condition on all clock consumers of crystal clock. **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	Clock Gating of CLKOUT_ITPxDP Disable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable dynamic control of CLKOUT_ITPxDP.When enabled, CLKOUT_ITPxDP is subject to gating/ ungating control by CPUBCLKREQ **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled

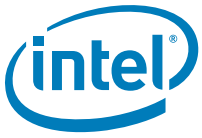


Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 12 of 13)

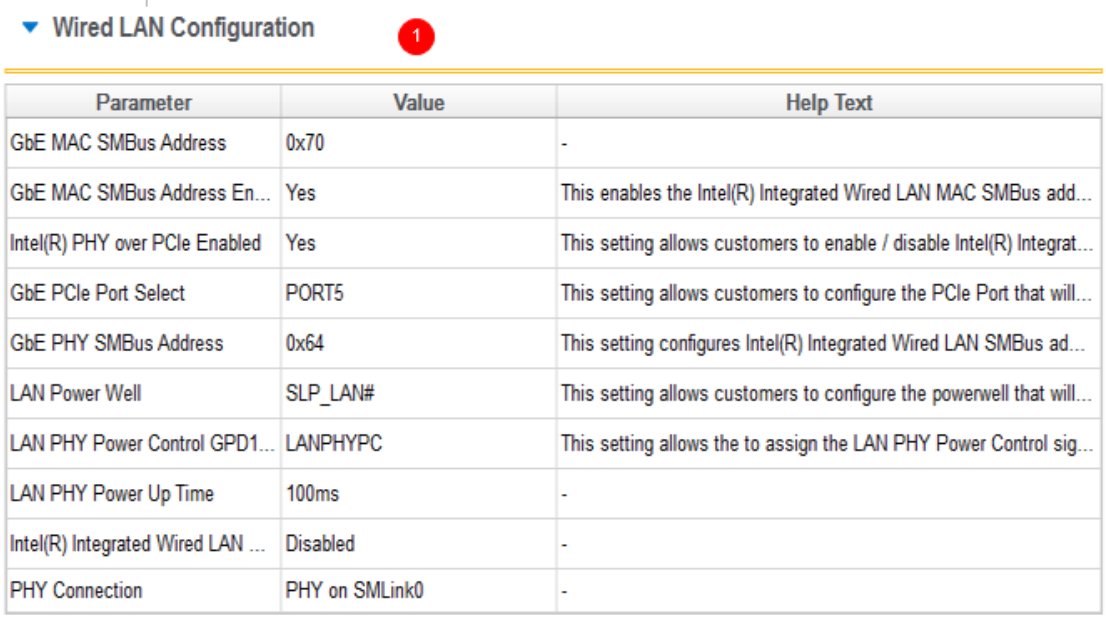
#	Parameter	Platform	Settings
	Clock Gating of CLKOUT_CPUBCLK Disable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable dynamic control of CLKOUT_CPUBCLK.When enabled, CLKOUT_CPUBCLK is subject to gating/ ungating control by CPUBCLKREQ These settings should match with platform hardware design. **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	Clock Gating of CLKOUT_CPUPCIBCLK Disable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable dynamic control of CLKOUT_CPUPCIBCLK.When enabled,CLKOUT_CPUPCIBCLK is subject to gating/ungating control by CPUPCIBCLKREQ **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	Clock Gating of CLKOUT_CPUNSSC Disable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable dynamic control of CLKOUT_CPUNSSC.When enabled,CLKOUT_CPUNSSC is subject to gating/ ungating control by CPUNSSCCLKREQ **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	Clock Gating of CLKOUT_CPUNSSC[P/N] Disable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable dynamic control of CLKOUT_CPUNSSC[P/N] .Controls the parked state of True (P) and Complementary (N) copies of the differential pair when CLKOUT_CPUNSSC[P/N] is dynamically gated under S0 idle state. **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	Clock Gating of icc_rosc_fast_clk Disable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable dynamic clock gate on icc_rosc_fast_clk **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	Clock Gating of icc_rosc_side_clk Disable **Values: Enabled / Disabled** This parameter allows user to Enable/Disable dynamic clock gate on icc_rosc_side_clk **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	USB3Gen2PCIe PLL OFF Wait This parameter allows user to set G2PLLOFFWAIT timer value. Once timer expires and there are no wake events, the USB3Gen2PCIe PLL can be shutdown **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	8us 8us 8us 8us
	USB3Gen2PCIe PLL PG Wait This parameter allows user to set G2PLLPGWAIT timer value. Once timer expires and there are no wake events, the USB3Gen2PCIe PLL can be shutdown **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	8us 8us 8us 8us
	Run-time S0 SUS PG Wait This parameter allows user to set SUSPGWAIT timer value. Once timer expires and there are no wake events, the USB3Gen2PCIe PLL can be shutdown **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	8us 8us 8us 8us

Table 2-8. Intel® FIT - Integrated Clock Controller (Sheet 13 of 13)

#	Parameter	Platform	Settings
	Crystal Oscillator Fast Restart Mode This parameter allows user to configure Crystal Oscillator Fast Restart Mode. In all below listed fast start modes, iSCLK kickstarts crystal XIN/ XOUT by injecting a 24Mhz kickstart reference clock onto these pins. **Note:** Configuration of this parameter co-relates to configuration of **Clock Gating of Core 24MHz Crystal Disable parameter.** If Clock Gating of Core 24MHz Crystal Disable is set to **'Disable'**, Crystal Oscillator Fast Restart Mode parameter has **no impact.** If Clock Gating of Core 24MHz Crystal Disable is set to **'Enabled'**, Crystal Oscillator Fast Restart Mode parameter **must be set to '01b'**. Other value like '00b' can cause wake latency conflict which can cause platform functional issue.	SKL-Y SKL-U SKL-H SKL-S	01b 01b 01b 01b
	BCLK PLL Shutdown Wait Interval This parameter allows user to enable Dynamic power management of BCLK PLL. Upon the event that all conditions (other than this wait timer itself) are satisfied for iSCLK dynamic PLL shutdown, a timer is started.Once it expires and there are no wake events, this PLL will shutdown. **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	8us 8us 8us 8us
	24MHz Crystal Shutdown Wait Interval This parameter allows user to Enable Dynamic power management of Crystal. Upon the event that all conditions (other than this wait timer itself) are satisfied for iSCLK crystal shutdown, a timer is started. Once it expires and there are no wake events, iSCLK will shutdown crystal. **Note:** Recommendation is to leave setting at default value.	SKL-Y SKL-U SKL-H SKL-S	8us 8us 8us 8us

Table 2-9. Intel® FIT - Intel® Networking & Connectivity (Sheet 1 of 3)

Click on Networking & Connectivity in the left tabs menu> Wired LAN Configuration is expanded by default:

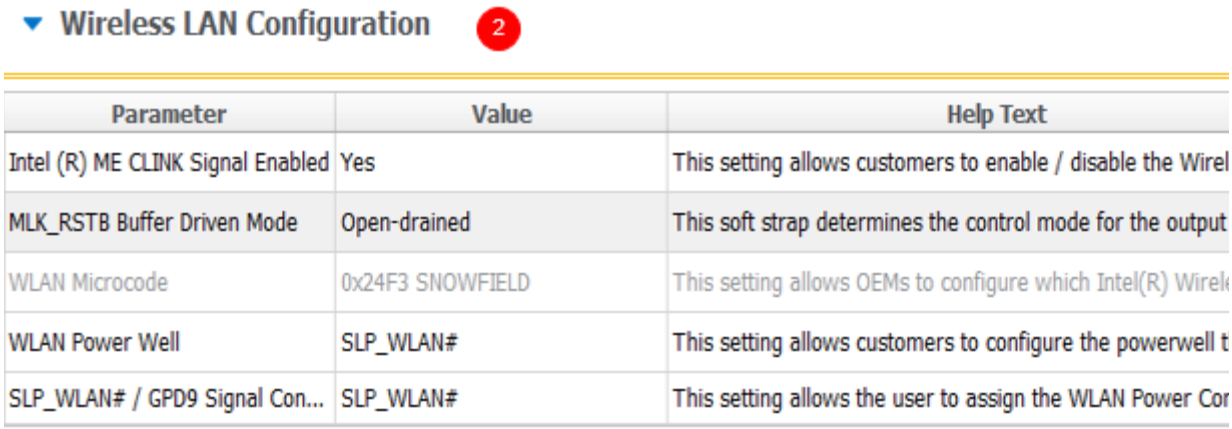


#	Parameter	Platform	Settings
1	**Networking & Connectivity - Wired LAN Configuration**		
	GbE MAC SMBus Address	SKL-Y SKL-U SKL-H SKL-S	0x70 0x70 0x70 0x70
	GbE SMBus Address Enabled **Values: Yes / No** - This enables the Intel® Integrated Wired LAN MAC SMBus address. **Note:** This setting must be enabled if using Intel® Integrated LAN.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	Intel® PHY over PCIe Enabled **Values: Yes / No** - This setting allows customers to enable / disable Intel® Integrated LAN operation over the PCIe Port selected by the GbE PCIe Port Select option.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	GbE PCIe Port Select **Values: PORT3, PORT4, PORT5, PORT9, PORT10** - This setting allows customers to configure the PCIe Port that will Intel® Integrated LAN will operate on.	SKL-Y SKL-U SKL-H SKL-S	PORT5 PORT4 PORT5 PORT5
	GbE PHY SMBus Address This setting configures Intel® Integrated Wired LAN SMBus address to accept SMBus cycles from the MAC. **Note:** Recommended setting is 64h.	SKL-Y SKL-U SKL-H SKL-S	0x64 0x64 0x64 0x64
	LAN Power Well **Values: Core Well, Sus Well, ME Well, SLP_LAN** - This setting allows customers to configure the power well that will be used by Intel® Integrated LAN. **Note:** Recommended setting is SLP_LAN#.	SKL-Y SKL-U SKL-H SKL-S	SLP_LAN# SLP_LAN# SLP_LAN# SLP_LAN#

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Table 2-9. Intel® FIT - Intel® Networking & Connectivity (Sheet 2 of 3)

#	Parameter	Platform	Settings
	LAN PHY Power Control GPD11 Signal Configuration **Values: GPD11, LANPHYPC -** This setting allows the customer to assign the LAN PHY Power Control signal to GbE or as GDP11. **Note:** If using Intel® Integrated LAN this setting should be set to "Enable as LANPHYPC".	SKL-Y SKL-U SKL-H SKL-S	LANPHYPC LANPHYPC LANPHYPC LANPHYPC
	LAN PHY Power Up Time **Values: 50ms, 100ms**	SKL-Y SKL-U SKL-H SKL-S	100ms 100ms 100ms 100ms
	Intel® Integrated Wired LAN Enable **Values: Enabled / Disabled -** This setting enables or disables the Intel® Integrated LAN.	SKL-Y SKL-U SKL-H SKL-S	Enabled Enabled Enabled Enabled
	PHY Connection **Values: No PHY connected, PHY on SMLink0**	SKL-Y SKL-U SKL-H SKL-S	PHY on SMLink0 PHY on SMLink0 PHY on SMLink0 PHY on SMLink0
Click on Networking & Connectivity in the left tabs menu> Wireless LAN Configuration is expanded by default:			

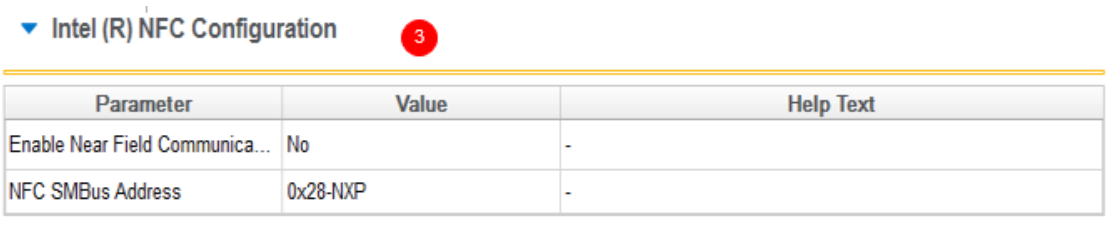


#	Parameter	Platform	Settings
2	**Networking & Connectivity - Wireless LAN Configuration**		
	CLINK Enabled **Values: Yes / No** - This setting allows customers to enable / disable the Wireless LAN CLINK signal through Intel® ME firmware. **Note:** For using Intel® vPro™ Wireless solutions this should be set to "Yes".	SKL-Y SKL-U SKL-H SKL-S	No No No No
	MLK_RSTB Buffer Driven Mode **Values: Open-drained / Driven** - This soft strap determines the control mode for the output buffer MLK_RST # signal.	SKL-Y SKL-U SKL-H SKL-S	NA NA Driven Driven
	WLAN Microcode - This setting allow OEMs to configure which Intel® Wireless LAN card microcode to load into the firmware image.	SKL-Y SKL-U SKL-H SKL-S	0x24F3 0x24F3 0x24F3 0x24F3

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Table 2-9. Intel® FIT - Intel® Networking & Connectivity (Sheet 3 of 3)

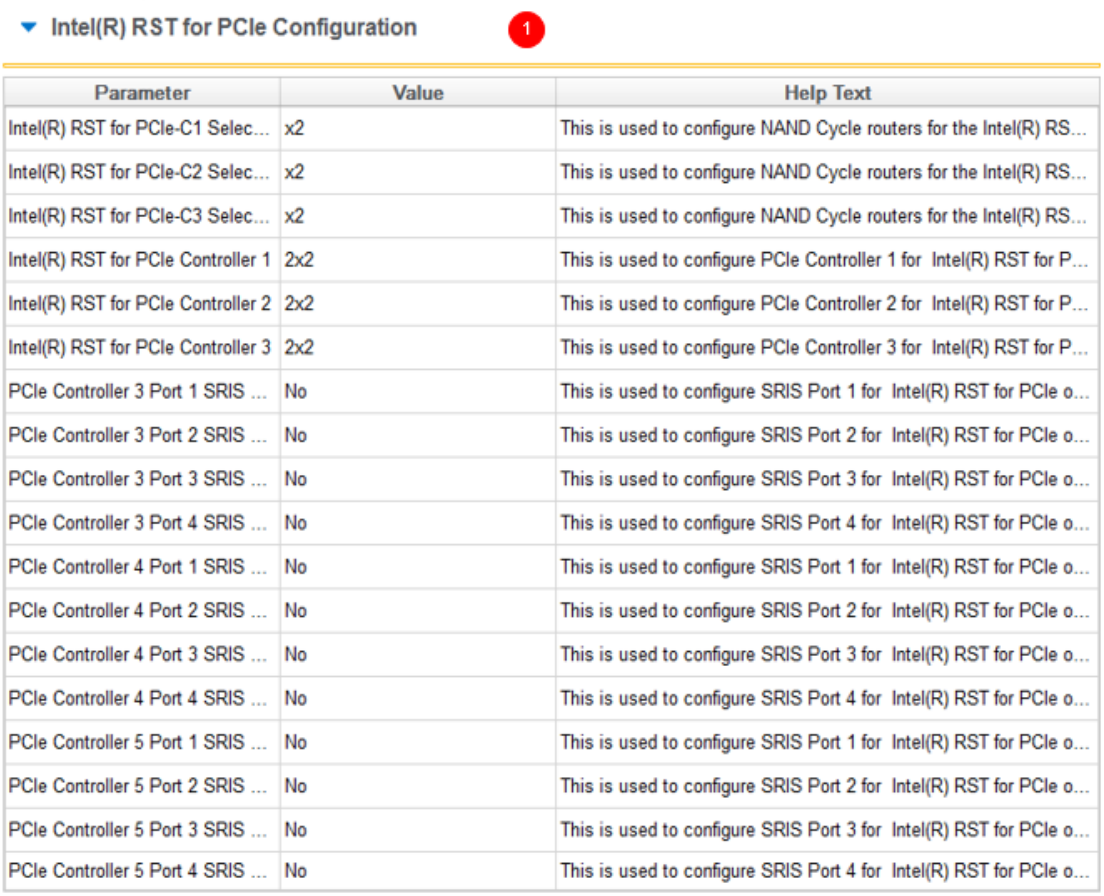
#	Parameter	Platform	Settings
	WLAN Power Well **Values: Disabled, Sus Well, ME Well, SLP_M#||SPDA, SLP_WLAN#** - This setting allows OEMs to configure the power well that will be used by Intel® Wireless LAN. WLAN Sleep via SLP_WLAN# (default) **Note:** Recommended setting is SLP_WLAN#.	SKL-Y SKL-U SKL-H SKL-S	SLP_WLAN# SLP_WLAN# SLP_WLAN# SLP_WLAN#
	SLP_WLAN# / GPD9 Signal Configuration **Values: SLP_WLAN#, GPD9** - This setting allows the customer to assign the WLAN Power Control signal to WLAN or as GDP9. **Note:** If using Intel® Wireless LAN this setting should be set to "Enable as SLP_WLAN#".	SKL-Y SKL-U SKL-H SKL-S	SLP_WLAN# SLP_WLAN# SLP_WLAN# SLP_WLAN#
Click on Networking & Connectivity in the left tabs menu> Intel® NFC Configuration is expanded by default:			



#	Parameter	Platform	Settings
3	**Networking & Connectivity Intel® NFC Configuration**		
	Enable Near Field Communication **Values: Yes/No** - This setting allows OEMs to enable / disable Near Field Communication support in the Intel® ME firmware. **Note:** If NFC device is not in the system configuration, leave this setting set to No, as it can cause BIST testing to fail.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes No No
	NFC SMBus Address **Values: 0x28-NXP, 0x29-NXP, 0x2A-NXP, 0x2B-NXP** - This setting allows OEMs to configure the SMBus address for the NFC adapter being used.	SKL-Y SKL-U SKL-H SKL-S	0x29-NXP 0x29-NXP 0x28-NXP 0x29-NXP

Table 2-10. Intel® FIT - Flex I/O (Sheet 1 of 10)

Click on Flex I/O in the left tabs menu> Intel® RST for PCIe Configuration is expanded by default:



#	Parameter	Platform	Settings
1	**Flex I/O - Intel® RST for PCIe Configuration**		
	Intel® RST for PCIe-C1 Select x2 or x4 **Values: x2, x4** - This is used to configure NAND Cycle routers for the Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe Controller 1.	SKL-Y SKL-U SKL-H SKL-S	NA NA x2 x2
	Intel® RST for PCIe-C2 Select x2 or x4 **Values: x2, x4** - This is used to configure NAND Cycle routers for the Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe Controller 2.	SKL-Y SKL-U SKL-H SKL-S	x2 x2 x2 x2
	Intel® RST for PCIe-C3 Select x2 or x4 **Values: x2, x4** - This is used to configure NAND Cycle routers for the Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe Controller 3.	SKL-Y SKL-U SKL-H SKL-S	x2 x4 x4 x4

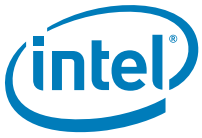


Table 2-10. Intel® FIT - Flex I/O (Sheet 2 of 10)

#	Parameter	Platform	Settings
	Intel® RST for PCIe Controller 1 **Values: 1x4, 2x2** - This is used to configure PCIe Controller 1 for Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe Controller 1.	SKL-Y SKL-U SKL-H SKL-S	NA NA x2 x2
	Intel® RST for PCIe Controller 2 **Values: 1x4, 2x2** - This is used to configure PCIe Controller 2 for Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe Controller 2.	SKL-Y SKL-U SKL-H SKL-S	x2 x2 x2 x2
	Intel® RST for PCIe Controller 3 **Values: 1x4, 2x2** - This is used to configure PCIe Controller 3 for Intel® RST for PCIe interface as either x2 or x4 lane operation on PCIe Controller 3.	SKL-Y SKL-U SKL-H SKL-S	x2 x4 x4 x4
	PCIe Controller 2 Port 1 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 1 for Intel® RST for PCIe on PCIe Controller 2. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 2 Port 2 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 2 for Intel® RST for PCIe on PCIe Controller 2.**Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 2 Port 3 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 3 for Intel® RST for PCIe on PCIe Controller 2. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 2 Port 4 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 4 for Intel® RST for PCIe on PCIe Controller 2. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 3 Port 1 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 1 for Intel® RST for PCIe on PCIe Controller 3. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 3 Port 2 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 2 for Intel® RST for PCIe on PCIe Controller 3. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 3 Port 3 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 3 for Intel® RST for PCIe on PCIe Controller 3. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 3 Port 4 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 4 for Intel® RST for PCIe on PCIe Controller 3. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 4 Port 1 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 1 for Intel® RST for PCIe on PCIe Controller 4. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
	PCIe Controller 4 Port 2 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 2 for Intel® RST for PCIe on PCIe Controller 4. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No

Table 2-10. Intel® FIT - Flex I/O (Sheet 3 of 10)

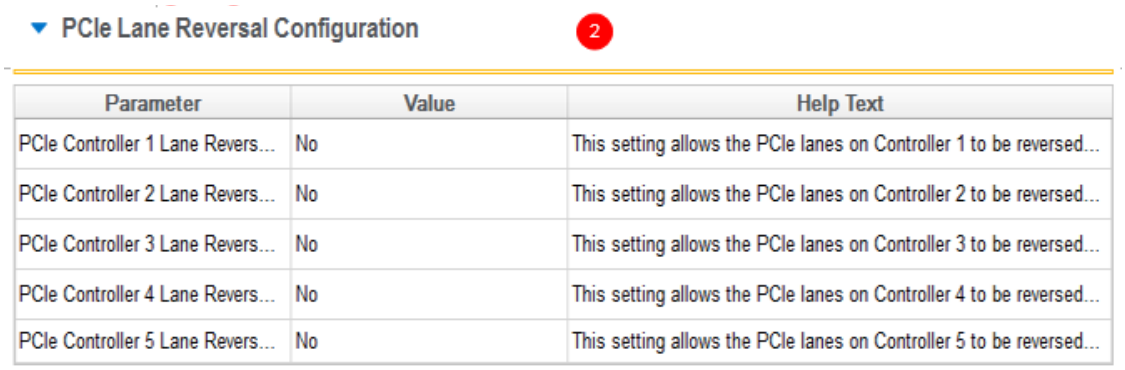
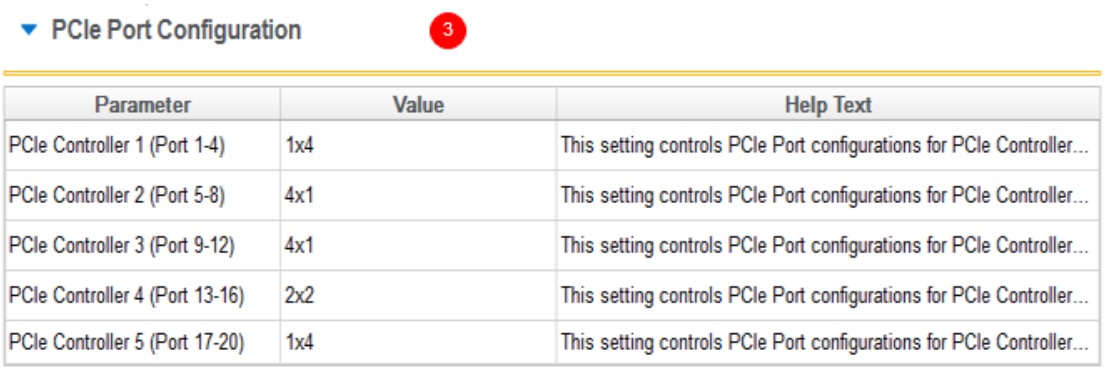
#	Parameter	Platform	Settings
	PCIe Controller 4 Port 3 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 3 for Intel® RST for PCIe on PCIe Controller 4. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
	PCIe Controller 4 Port 4 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 4 for Intel® RST for PCIe on PCIe Controller 4. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
	PCIe Controller 5 Port 1 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 1 for Intel® RST for PCIe on PCIe Controller 5. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
	PCIe Controller 5 Port 2 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 2 for Intel® RST for PCIe on PCIe Controller 5. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
	PCIe Controller 5 Port 3 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 3 for Intel® RST for PCIe on PCIe Controller 5. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
	PCIe Controller 5 Port 4 SRIS Enabled **Values: Yes/ No** - This is used to configure SRIS Port 4 for Intel® RST for PCIe on PCIe Controller 5. **Note:** Configuration of this setting is only required if the NVM device will be connected external SATA Express cable.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
Click on Flex I/O in the left tabs menu> PCIe Lane Reversal Configuration is expanded by default:			
		
#	**Parameter**	**Platform**	**Settings**
2	**Flex I/O - PCIe Lane Reversal Configuration**		
	PCIe Controller 1 Lane Reversal Enabled **Values: Yes/ No** - This setting allows the PCIe lanes on Controller 1 to be reversed. **Note:** In order to use Lane Reversal the PCIe Controller needs to be configured 1x4. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	PCIe Controller 2 Lane Reversal Enabled **Values: Yes/ No** - This setting allows the PCIe lanes on Controller 2 to be reversed. **Note:** In order to use Lane Reversal the PCIe Controller needs to be configured as 1x4. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	No No No No

Table 2-10. Intel® FIT - Flex I/O (Sheet 4 of 10)

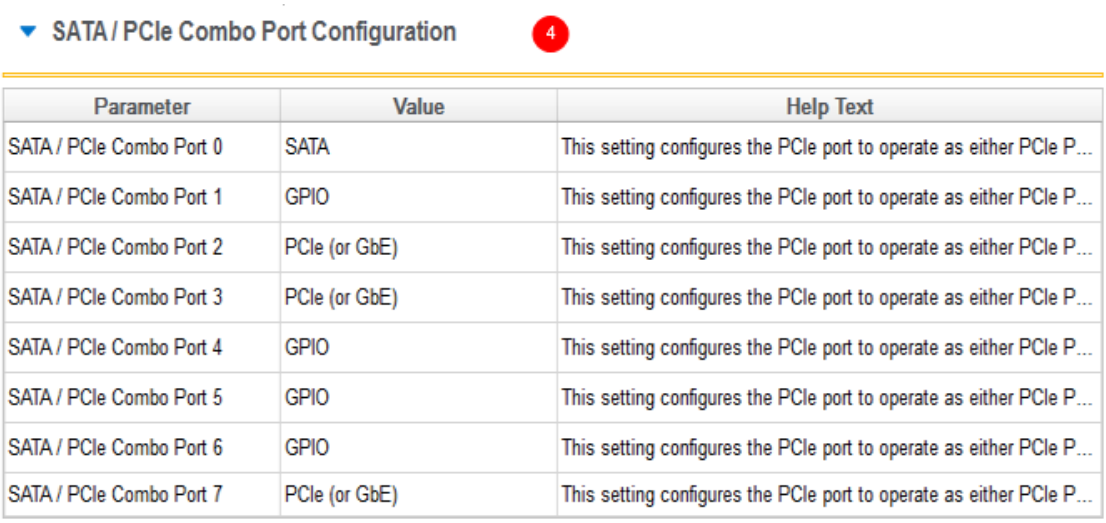
#	Parameter	Platform	Settings
	PCIe Controller 3 Lane Reversal Enabled **Values: Yes/ No** - This setting allows the PCIe lanes on Controller 3 to be reversed. **Note:** In order to use Lane Reversal the PCIe Controller needs to be configured as 1x4. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	No Yes No No
	PCIe Controller 4 Lane Reversal Enabled **Values: Yes/ No** - This setting allows the PCIe lanes on Controller 4 to be reversed. **Note:** In order to use Lane Reversal the PCIe Controller needs to be configured as 1x4. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
	PCIe Controller 5 Lane Reversal Enabled **Values: Yes/ No** - This setting allows the PCIe lanes on Controller 5 to be reversed. **Note:** In order to use Lane Reversal the PCIe Controller needs to be configured as 1x4. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No
Click on Flex I/O in the left tabs menu> PCIe Port Configuration is expanded by default:			



#	Parameter	Platform	Settings
3	**Flex I/O - PCIe Port Configuration**		
	PCIe Controller 1 (Port 1-4) **Values: 4x1, (1x2, 2x1), 2x2, 1x4** - This setting controls PCIe Port configurations for PCIe Controller 1. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	1x4 4x1 1x4 4x1
	PCIe Controller 2 (Port 5-8) **Values: 4x1, (1x2, 2x1), 2x2, 1x4** - This setting controls PCIe Port configurations for PCIe Controller 2. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	4x1 4x1 4x1 4x1
	PCIe Controller 3 (Port 9-12) **Values: 4x1, (1x2, 2x1), 2x2, 1x4** - This setting controls PCIe Port configurations for PCIe Controller 3. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	4x1 1x4 4x1 1x4
	PCIe Controller 4 (Port 13-16) **Values: 4x1, (1x2, 2x1), 2x2, 1x4** - This setting controls PCIe Port configurations for PCIe Controller 4. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA 1x2, 2x1 1x2, 2x1
	PCIe Controller 5 (Port 17-20) **Values: 4x1, (1x2, 2x1), 2x2, 1x4** - This setting controls PCIe Port configurations for PCIe Controller 5. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA 4x1 1x4

Table 2-10. Intel® FIT - Flex I/O (Sheet 5 of 10)

Click on Flex I/O in the left tabs menu> SATA / PCIe Combo Port Configuration is expanded by default:



#	Parameter	Platform	Settings
4	**Flex I/O - SATA / PCIe Combo Port Configuration**		
	SATA / PCIe Combo Port 0 **Values: SATA, PCIe (or GbE), GPIO** - This setting configures the PCIe port to operate as either: PCIe Port 7 or SATA Port 0 (LP) PCIe Port 9 or SATA Port 0 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	SATA SATA SATA PCIe (or GbE)
	SATA / PCIe Combo Port 1 **Values: SATA, PCIe (or GbE), GPIO** - This setting configures the PCIe port to operate as either: PCIe Port 8 or SATA Port 1 (LP) PCIe Port 10 or SATA Port 1 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	GPIO SATA SATA PCIe (or GbE)
	SATA / PCIe Combo Port 2 **Values: SATA, PCIe (or GbE), GPIO** - This setting configures the PCIe port to operate as either: PCIe Port 11 or SATA Port 1 (LP) PCIe Port 13 or SATA Port 0 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) SATA
	SATA / PCIe Combo Port 3 **Values: SATA, PCIe (or GbE), GPIO -** This setting configures the PCIe port to operate as either: PCIe Port 12 or SATA Port 2 (LP) PCIe Port 14 or SATA Port 1 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	PCIe (or GbE) PCIe (or GbE) PCIe (or GbE) SATA

Table 2-10. Intel® FIT - Flex I/O (Sheet 6 of 10)

#	Parameter	Platform	Settings
	SATA / PCIe Combo Port 4 **Values: SATA, PCIe (or GbE), GPIO -** This setting configures the PCIe port to operate as either: PCIe Port 15 or SATA Port 2 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) SATA
	SATA / PCIe Combo Port 5 **Values: SATA, PCIe (or GbE), GPIO -** This setting configures the PCIe port to operate as either: PCIe Port 16 or SATA Port 3 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) SATA
	SATA / PCIe Combo Port 6 **Values: SATA, PCIe (or GbE), GPIO -** This setting configures the PCIe port to operate as either: PCIe Port 17 or SATA Port 4 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) SATA
	SATA / PCIe Combo Port 7 **Values: SATA, PCIe (or GbE), GPIO -** This setting configures the PCIe port to operate as either: PCIe Port 18 or SATA Port 5 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) PCIe (or GbE)
	SATA / PCIe Combo Port 8 **Values: SATA, PCIe (or GbE), GPIO -** This setting configures the PCIe port to operate as either: PCIe Port 19 or SATA Port 6 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) PCIe (or GbE)
	SATA / PCIe Combo Port 9 **Values: SATA, PCIe (or GbE), GPIO -** This setting configures the PCIe port to operate as either: PCIe Port 20 or SATA Port 7 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) PCIe (or GbE)

Click on Flex I/O in the left tabs menu> SATA / PCIe Combo Port Select Polarity is expanded by default:

▼ SATA / PCIe Combo Port Select Polarity 5

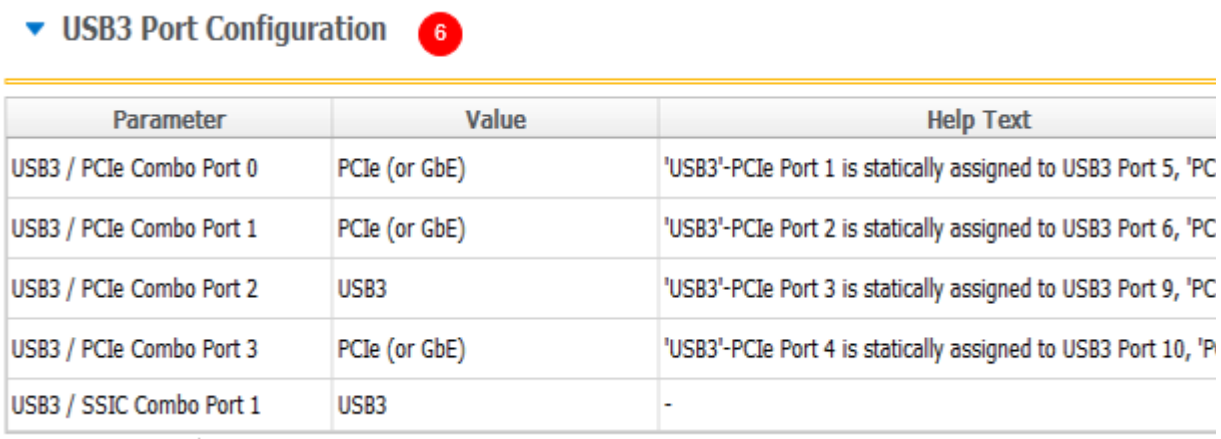
Parameter	Value	Help Text
Polarity Select SATA / PCIe Combo Port 0	0 = PCIe	This setting is used to determine the native mode con...
Polarity Select SATA / PCIe Combo Port 1	0 = PCIe	This setting is used to determine the native mode con...
Polarity Select SATA / PCIe Combo Port 2	0 = PCIe	This setting is used to determine the native mode con...
Polarity Select SATA / PCIe Combo Port 3	0 = PCIe	This setting is used to determine the native mode con...
Polarity Select SATA / PCIe Combo Port 4	0 = SATA	This setting is used to determine the native mode con...
Polarity Select SATA / PCIe Combo Port 5	0 = SATA	This setting is used to determine the native mode con...
Polarity Select SATA / PCIe Combo Port 6	0 = SATA	This setting is used to determine the native mode con...
Polarity Select SATA / PCIe Combo Port 7	0 = PCIe	This setting is used to determine the native mode con...

Table 2-10. Intel® FIT - Flex I/O (Sheet 7 of 10)

#	Parameter	Platform	Settings
5	**Flex I/O - SATA / PCIe Combo Port Select Polarity**		
	Polarity Select SATA / PCIe Combo Port 0 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 0. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	PCIe PCIe PCIe PCIe
	Polarity Select SATA / PCIe Combo Port 1 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 1. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	PCIe PCIe PCIe PCIe
	Polarity Select SATA / PCIe Combo Port 2 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 2. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	PCIe PCIe PCIe PCIe
	Polarity Select SATA / PCIe Combo Port 3 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 3. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	PCIe PCIe PCIe PCIe
	Polarity Select SATA / PCIe Combo Port 4 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 4. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA SATA PCIe
	Polarity Select SATA / PCIe Combo Port 5 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 5. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA SATA PCIe
	Polarity Select SATA / PCIe Combo Port 6 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 6. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA SATA PCIe
	Polarity Select SATA / PCIe Combo Port 7 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 7. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe PCIe
	Polarity Select SATA / PCIe Combo Port 8 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 8. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe PCIe
	Polarity Select SATA / PCIe Combo Port 9 **Values: 0 = SATA/0 = PCIe** - This setting is used to determine the native mode configuration for SATA / PCIe Combo Port 9. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe PCIe

Table 2-10. Intel® FIT - Flex I/O (Sheet 8 of 10)

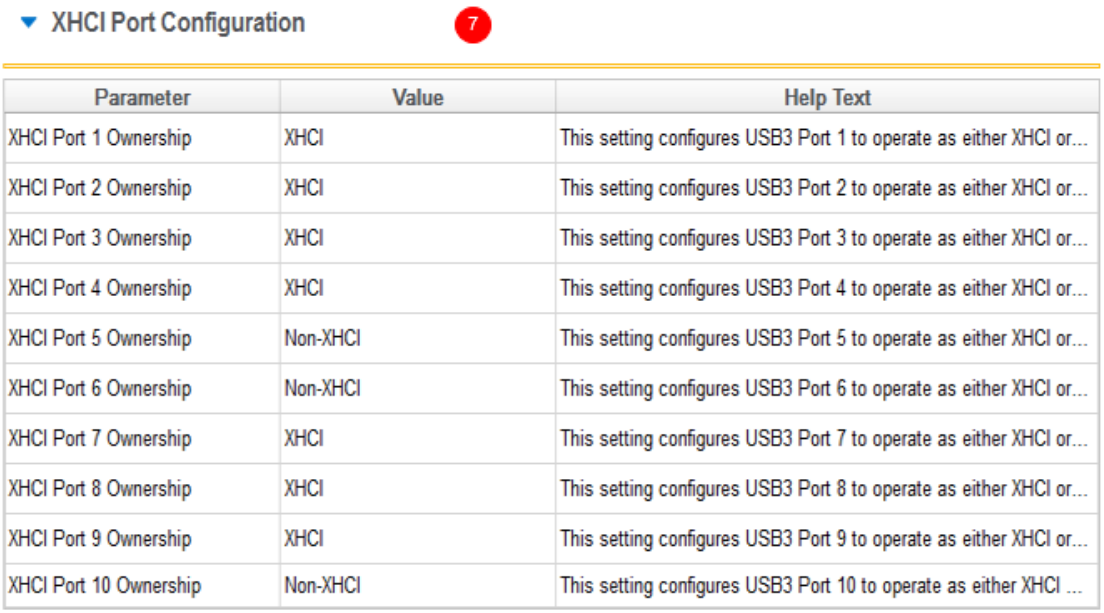
Click on Flex I/O in the left tabs menu> USB3 Port Configuration is expanded by default:



#	Parameter	Platform	Settings
6	**Flex I/O - USB3 Port Configuration**		
	USB3 / PCIe Combo Port 0 **Values: PCIe (or GbE), USB3 -** This setting configures the PCIe port to operate as either: PCIe Port 1 or USB3 Port 5 (LP) USB3 Port 7 or PCIe Port 1 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	PCIe (or GbE) USB3 PCIe (or GbE) USB3
	USB3 / PCIe Combo Port 1 **Values: PCIe (or GbE), USB3 -** This setting configures the PCIe port to operate as either: PCIe Port 6 or USB3 Port 2 (LP) USB3 Port 8 or PCIe Port 2 (H) For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	PCIe (or GbE) USB3 PCIe (or GbE) USB3
	USB3 / PCIe Combo Port 2 **Values: PCIe (or GbE), USB3** - This setting configures the PCIe port to operate as either USB3 Port 9 or PCIe Port 3. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA PCIe (or GbE) PCIe (or GbE)
	USB3 / PCIe Combo Port 3 **Values: PCIe (or GbE), USB3** - This setting configures the PCIe port to operate as either USB3 Port 10 or PCIe Port 4. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA USB3 USB3
	USB3 / SSIC Combo Port 1 **Values: USB3, SSIC** - This setting configures USB3 Port 1 to operate as either USB3 or SSIC. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	USB3 USB3 USB3 USB3

Table 2-10. Intel® FIT - Flex I/O (Sheet 9 of 10)

Click on Flex I/O in the left tabs menu> XHCI Port Configuration is expanded by default:



#	Parameter	Platform	Settings
7	**Flex I/O - XHCI Port Configuration**		
	XHCI Port 1 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 1 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	XHCI XHCI XHCI XHCI
	XHCI Port 2 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 2 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	XHCI XHCI XHCI XHCI
	XHCI Port 3 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 3 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	XHCI XHCI XHCI XHCI
	XHCI Port 4 Ownership **Values: XHCI, Non-XHCI -** - This setting configures USB3 Port 4 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	XHCI XHCI XHCI XHCI
	XHCI Port 5 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 5 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	Non-XHCI XHCI Non-XHCI XHCI
	XHCI Port 6 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 6 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	Non-XHCI XHCI Non-XHCI Non-XHCI

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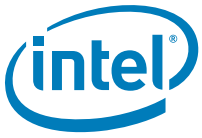
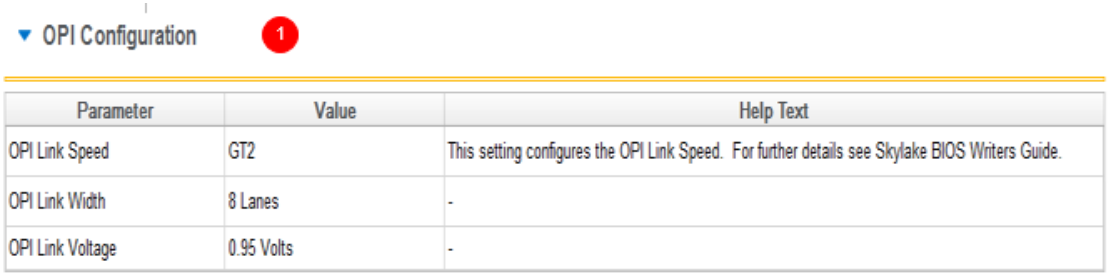


Table 2-10. Intel® FIT - Flex I/O (Sheet 10 of 10)

#	Parameter	Platform	Settings
	XHCI Port 7 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 7 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA XHCI XHCI
	XHCI Port 8 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 8 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA XHCI XHCI
	XHCI Port 9 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 9 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA XHCI XHCI
	XHCI Port 10 Ownership **Values: XHCI, Non-XHCI** - This setting configures USB3 Port 10 to operate as either XHCI or Non-XHCI. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	NA NA Non-XHCI Non-XHCI

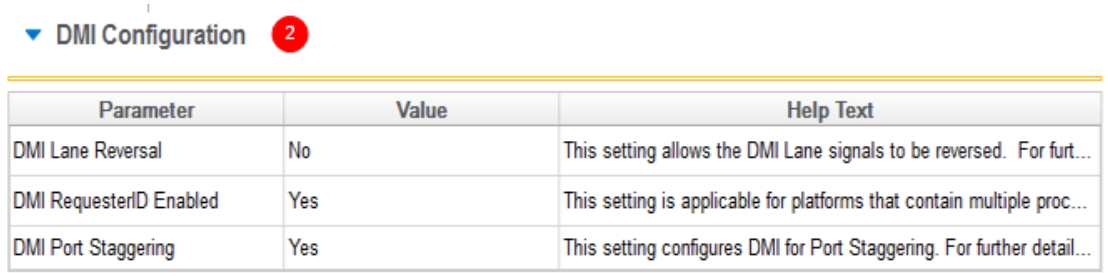
Table 2-11. Intel® FIT - Internal PCH Buses (Sheet 1 of 8)

Click on Internal PCH Buses in the left tabs menu> OPI Configuration is expanded by default:



#	Parameter	Platform	Settings
1	**Internal PCH Buses - OPI Configuration**	SKL-Y SKL-U SKL-H SKL-S	
	OPI Link Speed **Values: GT2 / GT4 -** This setting configures the OPI Link Speed. For further details see Skylake BIOS Writers Guide.	SKL-Y SKL-U SKL-H SKL-S	
	OPI Link Width **Values: 1 Lanes, 2 Lanes, 4 Lanes, 8 Lanes -** This setting configures the OPI Link Width. For further details see Skylake BIOS Writers Guide.	SKL-Y SKL-U SKL-H SKL-S	
	OPI Link Voltage **Values: 0.85 Volts, 0.95 Volts -** This setting configures the OPI Link Voltage. For further details see Skylake BIOS Writers Guide.	SKL-Y SKL-U SKL-H SKL-S	

Click on Internal PCH Buses in the left tabs menu> DMI Configuration is expanded by default:



#	Parameter	Platform	Settings
2	**Internal PCH Buses - DMI Configuration**		
	DMI Lane Reversal **Values: Yes / No** - This setting allows the DMI Lane signals to be reversed. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	DMI RequesterID Enabled **Values: Yes / No** - This setting is applicable for platforms that contain multiple processor sockets. If multiple processors need to access Serial Flash then this needs to be set to 'Yes'. If platform has only one processor socket set this to 'No'.	SKL-Y SKL-U SKL-H SKL-S	NA NA No No

Table 2-11. Intel® FIT - Internal PCH Buses (Sheet 2 of 8)

#	Parameter	Platform	Settings
	DMI Port Staggering **Values: Yes/No** - This setting configures DMI for Port Staggering. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes

Click on Internal PCH Buses in the left tabs menu> eSPI Configuration is expanded by default:

▼ eSPI Configuration 3

Parameter	Value	Help Text
eSPI / EC Boot Enabled	Yes	-
eSPI / EC Bus Frequency	60MHz	-
eSPI / EC CRC Check Enabled	Yes	-
eSPI / EC Max Outstanding R...	2	-
eSPI / EC Max Read Request ...	64 bytes	-
eSPI / EC Max Read Request ...	64 bytes	-
eSPI / EC Max Read Request ...	64 bytes	-
eSPI / EC Max Virtual Wire Ch...	8	-
eSPI / EC Maximum I/O Mode	Single, Dual and Quad	-
eSPI / EC OOB Channel Enabled	Yes	-
eSPI / EC Peripheral Channel ...	Yes	-
eSPI / EC Slave Device Max R...	Disabled	-
eSPI / EC Slave Device Max O...	2	-
eSPI / EC Slave Device Max R...	64 bytes	-
eSPI / EC Slave Device Max R...	64 bytes	-
eSPI / EC Slave Device OOB ...	Enabled	-
eSPI / EC Slave Device Periph...	Enabled	-
eSPI / EC Slave Device Virtual...	Enabled	-
eSPI / EC Slave Device CRC C...	Yes	-
eSPI / EC Slave Device Maxim...	Single	-
eSPI / EC Slave Device Bus Fr...	20MHz	-
eSPI / EC Slave Device Max V...	8	-
eSPI / EC Slave Device Enabled	Disabled	-

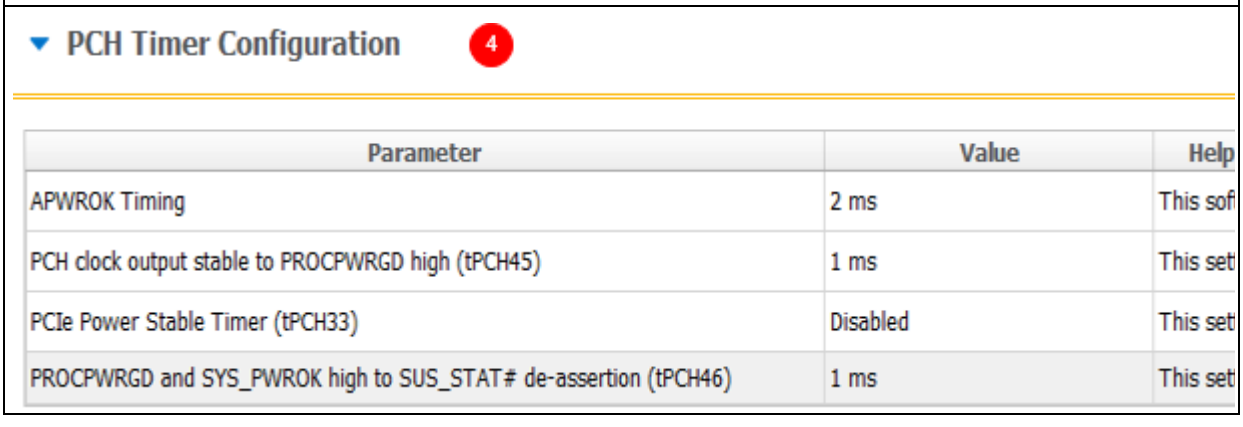
Table 2-11. Intel® FIT - Internal PCH Buses (Sheet 3 of 8)

#	Parameter	Platform	Settings
3	**Internal PCH Buses - eSPI Configuration**		
	eSPI / EC Boot Enabled **Values: Yes/No**	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	eSPI / EC Bus Frequency **20MHz, 24MHz, 30MHz, 40MHz, 60MHz**	SKL-Y SKL-U SKL-H SKL-S	60MHz 60MHz 60MHz 60MHz
	eSPI / EC CRC Check Enabled **Values: Yes/No**	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes No
	eSPI / EC Max Outstanding Requests for Master Attached Flash Channel **Values: 1, 2**	SKL-Y SKL-U SKL-H SKL-S	2 2 2 2
	eSPI / EC Max Read Request Payload size for Master Attached Flash Channel **Values: 64 bytes, 128 bytes, 256 bytes, 512 bytes, 1024 bytes, 2048 bytes, 4096 bytes**	SKL-Y SKL-U SKL-H SKL-S	64 bytes 64 bytes 64 bytes 64 bytes
	eSPI / EC Max Read Request Payload size for OOB Channel **Values: 64 bytes, 128 bytes, 256 bytes, 512 bytes, 1024 bytes, 2048 bytes, 4096 bytes**	SKL-Y SKL-U SKL-H SKL-S	64 bytes 64 bytes 64 bytes 64 bytes
	eSPI / EC Max Read Request Payload size for Peripheral Channel **Values: 64 bytes, 128 bytes, 256 bytes, 512 bytes, 1024 bytes, 2048 bytes, 4096 bytes**	SKL-Y SKL-U SKL-H SKL-S	64 bytes 64 bytes 64 bytes 64 bytes
	eSPI / EC Max Virtual Wire Channels **Values: 8, 4, 2, 1**	SKL-Y SKL-U SKL-H SKL-S	8 8 8 8
	eSPI / EC Maximum I/O Mode **Values: Single, Single and Dual, Single and Quad, Single Dual and Quad**	SKL-Y SKL-U SKL-H SKL-S	Single, Dual and Quad Single, Dual and Quad Single, Dual and Quad Single, Dual and Quad
	eSPI / EC OOB Channel Enabled **Values: Yes/No**	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	eSPI / EC Peripheral Channel Enabled **Values: Yes/No**	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	eSPI / EC Slave Device Max Read Request OOB Channel Enable **Values: Enabled/Disabled**	SKL-Y SKL-U SKL-H SKL-S	NA NA Disabled Disabled
	eSPI / EC Slave Device Max Outstanding Requests	SKL-Y SKL-U SKL-H SKL-S	NA NA 2 2

Table 2-11. Intel® FIT - Internal PCH Buses (Sheet 4 of 8)

#	Parameter	Platform	Settings
	eSPI / EC Slave Device Max Read Request Payload size for OOB Channel	SKL-Y SKL-U SKL-H SKL-S	64 bytes 64 bytes 64 bytes 64 bytes
	eSPI / EC Slave Device Max Read Request Payload size for Peripheral Channel	SKL-Y SKL-U SKL-H SKL-S	64 bytes 64 bytes 64 bytes 64 bytes
	eSPI / EC Slave Device OOB Channel Enable **Values: Enabled / Disabled**	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	eSPI / EC Slave Device Peripheral Channel Enable **Values: Enabled / Disabled**	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	eSPI / EC Slave Device Virtual Wire Channel Enabled **Values: Enabled / Disabled**	SKL-Y SKL-U SKL-H SKL-S	NA NA Enabled Enabled
	eSPI / EC Slave Device CRC Check Enabled **Values: Yes / No**	SKL-Y SKL-U SKL-H SKL-S	NA NA Yes Yes
	eSPI / EC Slave Device Maximum I/O Mode	SKL-Y SKL-U SKL-H SKL-S	NA NA Single Single
	eSPI / EC Slave Device Bus Frequency	SKL-Y SKL-U SKL-H SKL-S	NA NA 20MHz 20MHz
	eSPI / EC Slave Device Max Virtual Wire Channels	SKL-Y SKL-U SKL-H SKL-S	NA NA 8 8
	eSPI / EC Slave Device Enabled **Values: Enabled / Disabled**	SKL-Y SKL-U SKL-H SKL-S	NA NA Disabled Disabled

Click on Internal PCH Buses in the left tabs menu> PCH Timer Configuration is expanded by default:



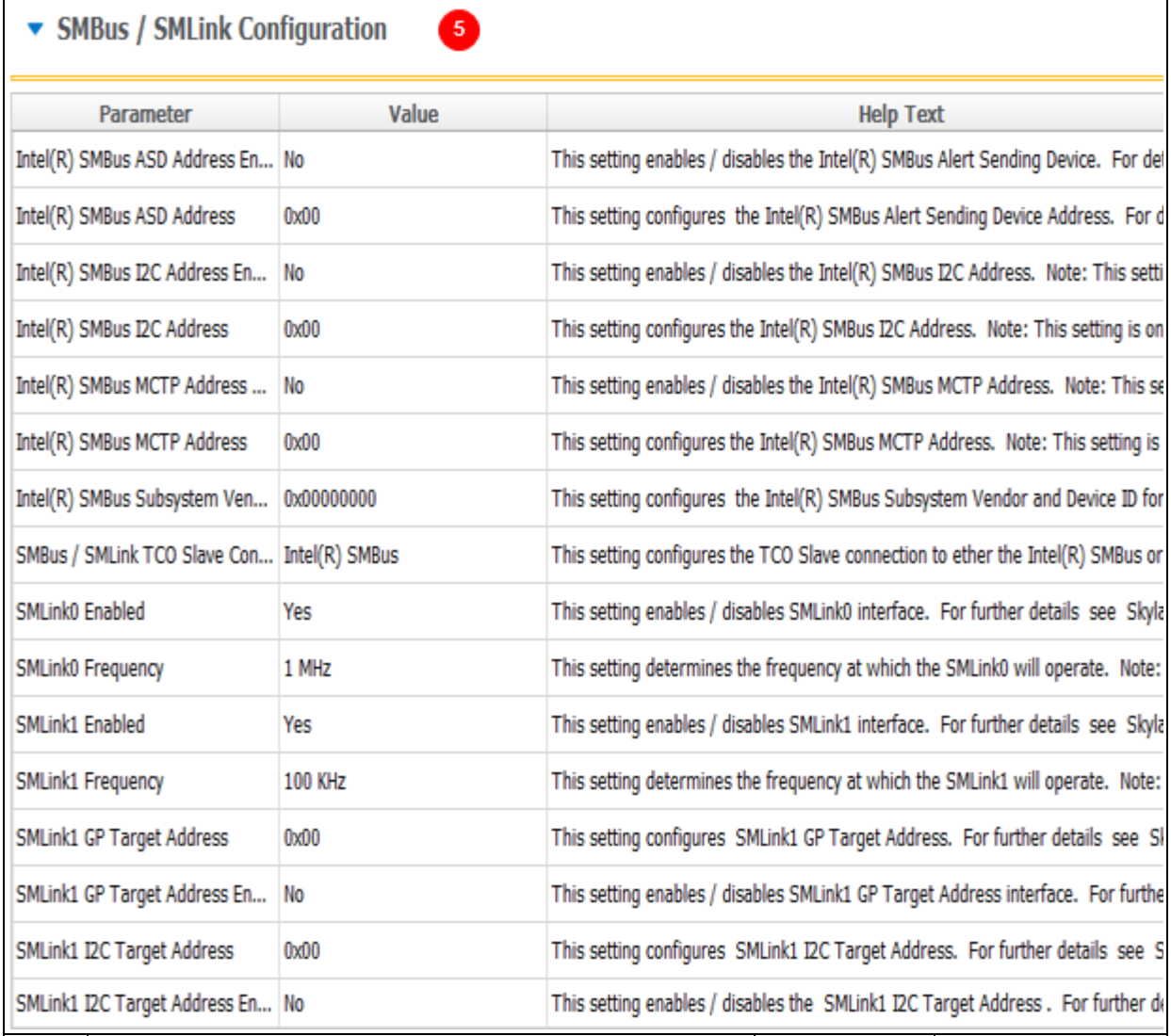
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Table 2-11. Intel® FIT - Internal PCH Buses (Sheet 5 of 8)

#	Parameter	Platform	Settings
4	**Internal PCH Buses - PCH Timer Configuration**		
	APWROK Timing **Values: 2ms, 4ms, 8ms, 16ms** - This soft strap determines the time between the SLP_A# pin de-asserting and the APWROK timer expiration. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	2 ms 2 ms 2 ms 2 ms
	PCH clock output stable to PROCPWRGD high (tPCH45) **Values: 100ms, 50ms, 5ms, 1ms** - This setting configures the minimum timing from XCK_PLL locked to CPUPWRGD high. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	1 ms 1 ms 1 ms 1 ms
	PCIe Power Stable Timer (tPCH33) **Values: Enabled/Disabled** - This setting configures the enables / disables the t36 timer. When enabled PCH will count 99ms from PWROK assertion before PLTRST# is de-asserted. **Note:** The recommended setting is "Disabled".	SKL-Y SKL-U SKL-H SKL-S	Disabled Disabled Disabled Disabled
	PROCPWRGD and SYS_PWROK high to SUS_STAT# de-assertion (tPCH46) **Values: 1ms, 2ms, 5ms** - This setting configures the minimum timing from CPUPWRGD assertion to SUS_STAT#. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	1 ms 1 ms 1 ms 1 ms

Table 2-11. Intel® FIT - Internal PCH Buses (Sheet 6 of 8)

Click on Internal PCH Buses in the left tabs menu> SMBus / SMLink Configuration is expanded by default:



#	Parameter	Platform	Settings
5	**Internal PCH Buses - SMBus / SMLink Configuration**		
	Intel® SMBus ASD Address Enable **Values: Yes / No** - This setting enables / disables the Intel® SMBus Alert Sending Device. For details see Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Intel® SMBus ASD Address - This setting configures the Intel® SMBus Alert Sending Device Address. For details see Skylake H / LP SPI Programming guide for further details.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000

Table 2-11. Intel® FIT - Internal PCH Buses (Sheet 7 of 8)

#	Parameter	Platform	Settings
	Intel® SMBus I2C Address Enabled **Values: Yes/No** - This setting enables / disables the Intel® SMBus I2C Address. Note: This setting is only used for testing purposes. The recommended setting is "No".	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Intel® SMBus I2C Address - This setting configures the Intel® SMBus I2C Address. **Note:** This setting is only used for testing purposes. The recommended setting is "0000000".	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
	Intel® SMBus MCTP Address Enabled **Values: Yes/No** - This setting enables / disables the Intel® SMBus MCTP Address. **Note:** This setting is only used for testing purposes. The recommended setting is "No".	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Intel® SMBus MTCP Address - This setting configures the Intel® SMBus MCTP Address. **Note:** This setting is only used for testing purposes. The default setting is "0000000".	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
	Intel® SMBus Subsystem Vendor & Device ID for ASF - This setting configures the Intel® SMBus Subsystem Vendor & Device ID for ASF. For details see Skylake H / LP SPI Programming guide further details.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
	SMBus / SMLink TCO Slave Connection **Values: Intel® SMBus, SMLink0** - This setting configures the TCO Slave connection to ether the Intel® SMBus or SMLink0. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	Intel® SMBus Intel® SMBus Intel® SMBus Intel® SMBus
	SMLink0 Enabled **Values: Yes/No** - This setting enables / disables SMLink0 interface. For further details see Skylake H / LP Platform Controller Hub EDS. **Note:** If using Intel® NFC this setting must be set to "Yes".	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	SMLink0 Frequency **Values: 100KHz, 400KHz, 1 MHz** - This setting determines the frequency at which the SMLink0 will operate. **Note:** The recommended setting is "1MHz".	SKL-Y SKL-U SKL-H SKL-S	1 MHz 1 MHz 1 MHz 1 MHz
	SMLink1 Enabled **Values: Yes/No** - This setting enables / disables SMLink1 interface. For further details see Skylake H / LP Platform Controller Hub EDS. **Note:** This setting must be set to "Yes" if using PCH / MCP Thermal reporting.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	SMLink1 Frequency **Values: 100KHz, 400KHz, 1 MHz** - This setting determines the frequency at which the SMLink1 will operate. **Note:** The recommended setting is "100KHz".	SKL-Y SKL-U SKL-H SKL-S	100 KHz 100 KHz 100 KHz 100 KHz
	SMLink1 GP Target Address - This setting configures SMLink1 GP Target Address. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
	SMLink1 GP Target Address Enabled **Values: Yes/No** - This setting enables / disables SMLink1 GP Target Address interface. For further details see Skylake H / LP Platform Controller Hub EDS. **Note:** This setting must be set to "Yes" if using PCH / MCP Thermal reporting.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	SMLink1 I2C Target Address - This setting configures SMLink1 I2C Target Address. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000

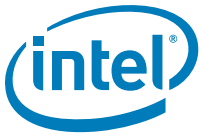


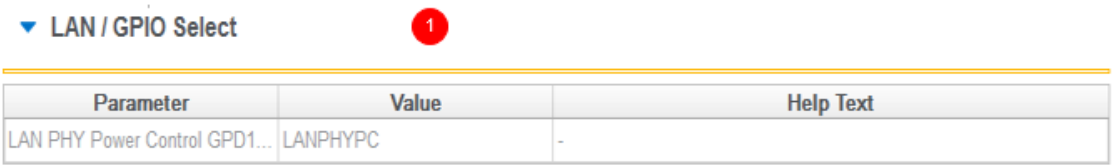
Table 2-11. Intel® FIT - Internal PCH Buses (Sheet 8 of 8)

#	Parameter	Platform	Settings
	SMLink1 I2C Target Address Enabled **Values: Yes / No** - This setting configures SMLink1 I2C Target Address. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	No No No No

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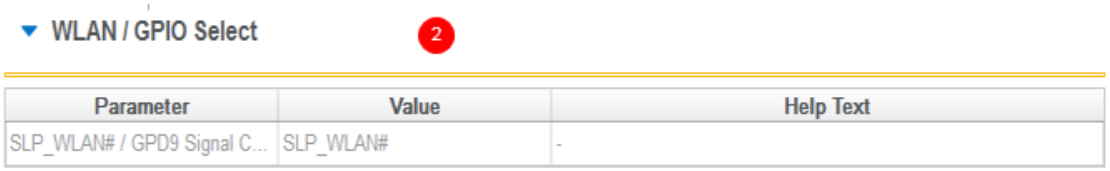
Table 2-12. Intel® FIT - GPIO (Sheet 1 of 2)

Click on GPIO in the left tabs menu> LAN / GPIO Select is expanded by default:



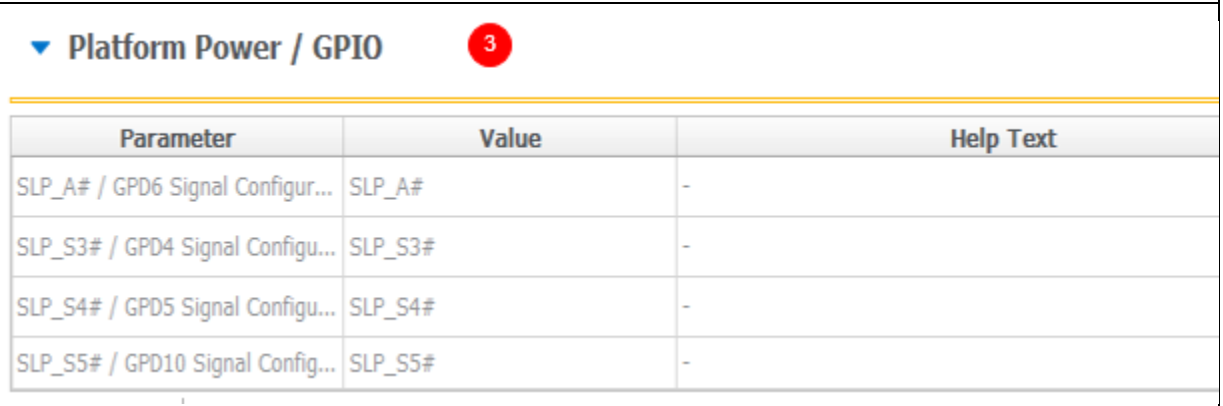
#	Parameter	Platform	Settings
1	**GPIO - LAN / GPIO Select**		
	LAN PHY Power Control GPD11 Signal Configuration	SKL-Y SKL-U SKL-H SKL-S	LANPHYPC LANPHYPC LANPHYPC LANPHYPC

Click on GPIO in the left tabs menu> WLAN / GPIO Select is expanded by default:



#	Parameter	Platform	Settings
2	**GPIO - WLAN / GPIO Select**		
	SLP_WLAN# / GPD9 Signal Configuration	SKL-Y SKL-U SKL-H SKL-S	SLP_WLAN# SLP_WLAN# SLP_WLAN# SLP_WLAN#

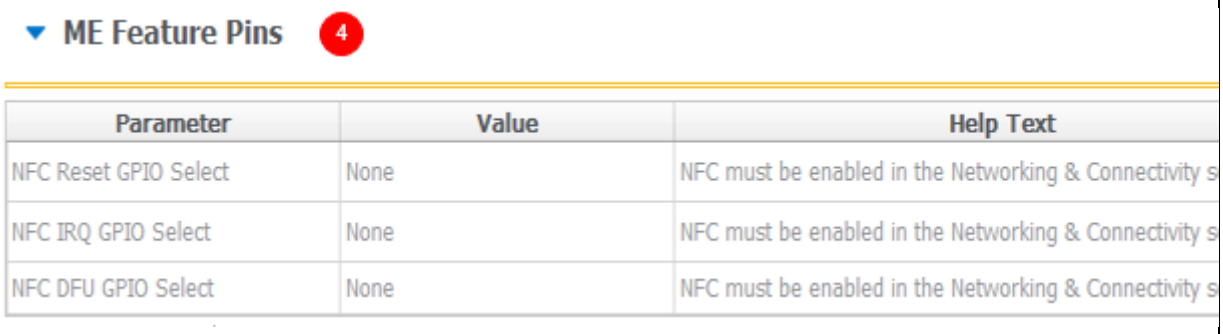
Click on GPIO in the left tabs menu> Platform Power / GPIO is expanded by default:



#	Parameter	Platform	Settings
3	**GPIO - Platform Power / GPIO**		

Table 2-12. Intel® FIT - GPIO (Sheet 2 of 2)

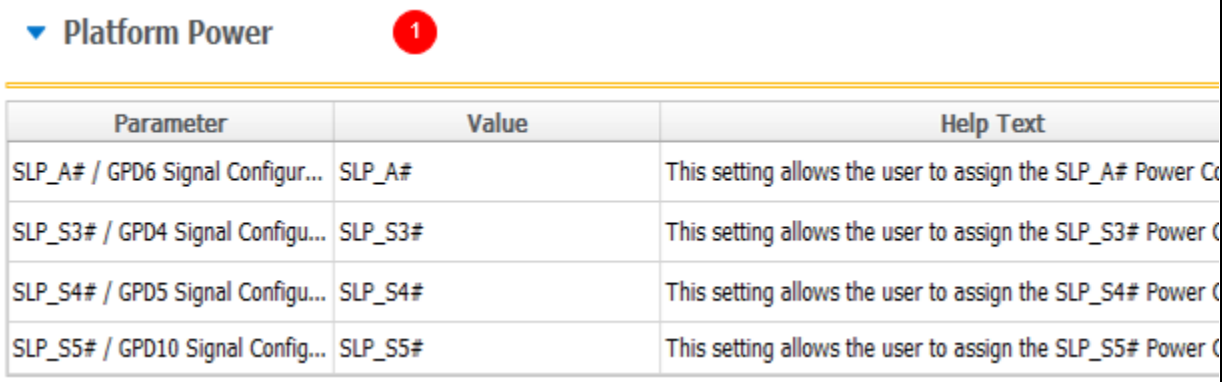
#	Parameter	Platform	Settings
	SLP_A# / GPD6 Signal Configuration	SKL-Y SKL-U SKL-H SKL-S	SLP_A# SLP_A# SLP_A# SLP_A#
	SLP_S3# / GPD4 Signal Configuration	SKL-Y SKL-U SKL-H SKL-S	SLP_S3# SLP_S3# SLP_S3# SLP_S3#
	SLP_S4# / GPD5 Signal Configuration	SKL-Y SKL-U SKL-H SKL-S	SLP_S4# SLP_S4# SLP_S4# SLP_S4#
	SLP_S5# / GPD10 Signal Configuration	SKL-Y SKL-U SKL-H SKL-S	SLP_S5# SLP_S5# SLP_S5# SLP_S5#
Click on GPIO in the left tabs menu> ME Feature Pins is expanded by default:			



#	Parameter	Platform	Settings
4	**GPIO - ME Feature Pins**		
	NFC Reset GPIO Select NFC must be enabled in the Networking and Connectivity section to configure this setting.		
	NFC IRQ GPIO Select NFC must be enabled in the Networking and Connectivity section to configure this setting.		
	NFC DFU GPIO Select NFC must be enabled in the Networking and Connectivity section to configure this setting.		

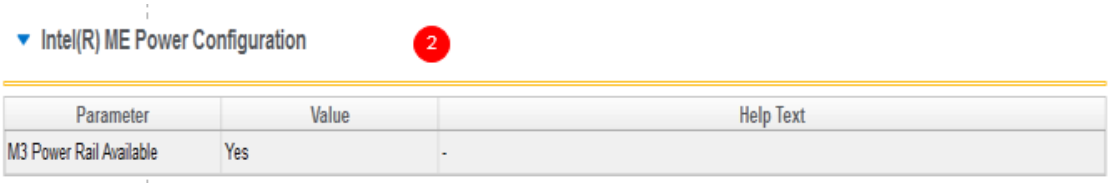
Table 2-13. Intel® FIT - Power (Sheet 1 of 2)

Click on Power in the left tabs menu> Platform Power is expanded by default:



#	Parameter	Platform	Settings
1	**Power - Platform Power**		
	SLP_A# / GPD6 Signal Configuration **Values: SLP_A#, GPD6** - This setting allows the customer to assign the SLP_A# Power Control signal as SLP_A# or as GDP6. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	SLP_A# SLP_A# SLP_A# SLP_A#
	SLP_S3# / GPD4 Signal Configuration **Values: SLP_S3#, GPD4** - This setting allows the customer to assign the SLP_S3# Power Control signal as SLP_S3# or as GDP4. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	SLP_S3# SLP_S3# SLP_S3# SLP_S3#
	SLP_S4# / GPD5 Signal Configuration **Values: SLP_S4#, GPD5** - This setting allows the customer to assign the SLP_S4# Power Control signal as SLP_S4# or as GDP5. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	SLP_S4# SLP_S4# SLP_S4# SLP_S4#
	SLP_S5# / GPD10 Signal Configuration **Values: SLP_S5#, GPD10** - This setting allows the customer to assign the SLP_S5# Power Control signal as SLP_S5# or as GDP10. For further details see Skylake H / LP Platform Controller Hub EDS.	SKL-Y SKL-U SKL-H SKL-S	SLP_S5# SLP_S5# SLP_S5# SLP_S5#

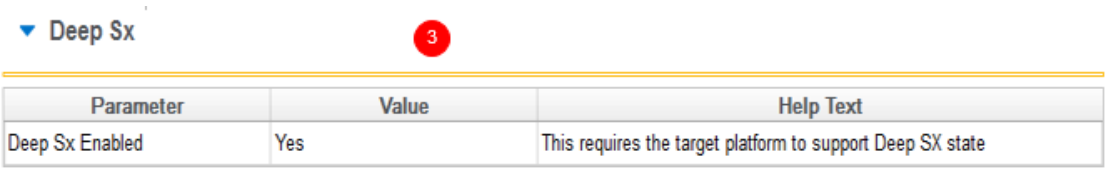
Click on Power in the left tabs menu> Intel® ME Power Configuration is expanded by default:



#	Parameter	Platform	Settings
2	**Power - Intel® ME Power Configuration**		
	M3 Power Rail Available **Values: Yes / No** - This setting enables / disables support for M3 operation of the firmware. **Note:** Support for M3 is dependent on HW board design. For Intel® vPro™ platform this setting must be set to "Yes".	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes

Table 2-13. Intel® FIT - Power (Sheet 2 of 2)

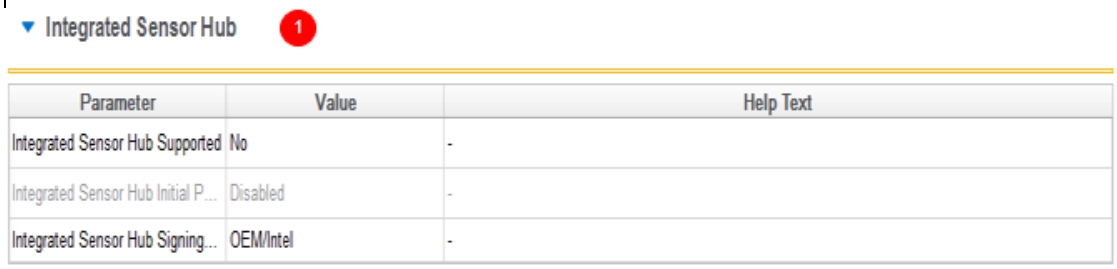
Click on Power in the left tabs menu> Deep Sx is expanded by default:



#	Parameter	Platform	Settings
3	**Power - Deep Sx**		
	Deep Sx Enabled **Values: Yes/ No -** This setting enables / disables support for Deep Sx operation. For further details see Skylake H / LP Platform Controller Hub EDS. **Note:** Support for Deep Sx is board design dependent.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes

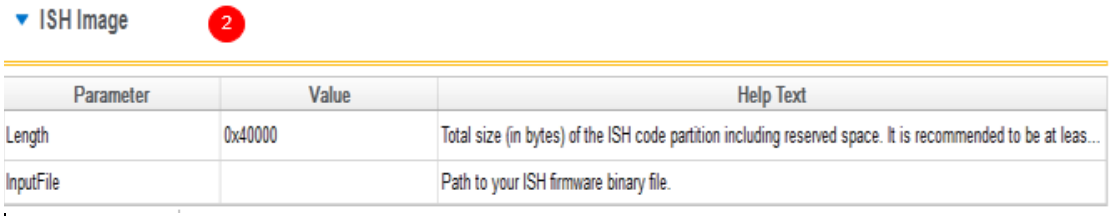
Table 2-14. Intel® FIT - Integrated Sensor Hub (Sheet 1 of 2)

Click on Integrated Sensor Hub in the left tabs menu> Integrated Sensor Hub is expanded by default:



#	Parameter	Platform	Settings
1	**Integrated Sensor Hub**		
	Integrated Sensor Hub Supported **Values: Yes / No** This setting allows customers to disable ISH on the platform.	SKL-Y SKL-U SKL-H SKL-S	
	Integrated Sensor Hub Power Up State **Values: Enabled / Disabled** Field is enabled for editing if "Integrated Sensor Hub Supported" field above is set to "Yes". This setting allows customers to determine the power up state for ISH.	SKL-Y SKL-U SKL-H SKL-S	
	Integrated Sensor Hub Signing Policy **Values: OEM / Intel, OEM** This setting determines ISH signing will be checked against the Intel provisioned hash included in the base image or OEM public key hash provisioned on the platform.	SKL-Y SKL-U SKL-H SKL-S	

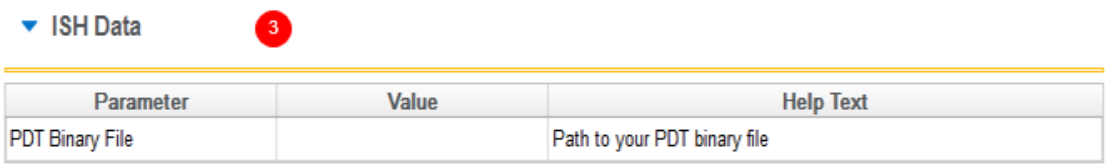
Click on Integrated Sensor Hub in the left tabs menu> ISH Image is expanded by default:



#	Parameter	Platform	Settings
2	**Integrated Sensor Hub - ISH Image**		
	Length - Total size (in bytes) of the ISH code partition including reserved space. It is recommended to be at least 256kb.		
	Input File	SKL-Y SKL-U SKL-H SKL-S	Path to your ISH firmware binary file Path to your ISH firmware binary file Path to your ISH firmware binary file Path to your ISH firmware binary file

Table 2-14. Intel® FIT - Integrated Sensor Hub (Sheet 2 of 2)

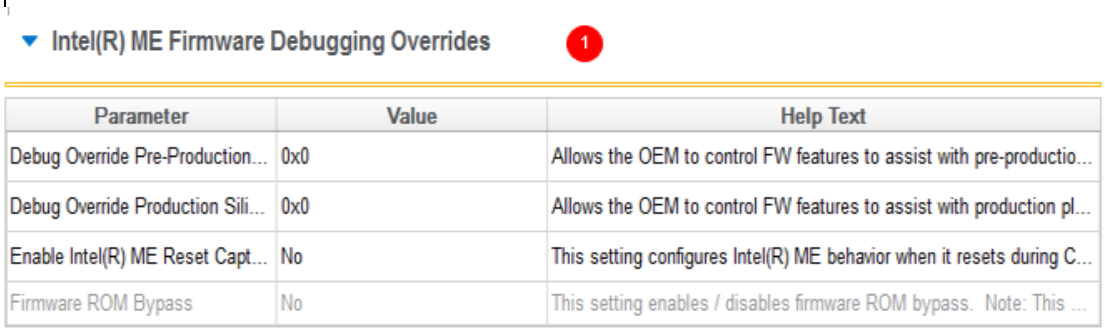
Click on Integrated Sensor Hub in the left tabs menu> ISH Data is expanded by default:



#	Parameter	Platform	Settings
3	**Integrated Sensor Hub - ISH Data**		
	PDT Binary File	SKL-Y SKL-U SKL-H SKL-S	Path for PDT Binary file Path for PDT Binary file Path for PDT Binary file Path for PDT Binary file

Table 2-15. Intel® FIT - Debug (Sheet 1 of 3)

Click on Debug in the left tabs menu> Intel® ME Firmware Debugging Overrides is expanded by default:



#	Parameter	Platform	Settings
1	**Debug - Intel® ME Firmware Debugging Overrides**		
	Debug Override Pre-Production Silicon - Allows the OEM to control FW features to assist with pre-production platform debugging. This control has no effect if used on production silicon. **Bit 0:** Disable DRAM_INIT_DONE (default timeout 60 seconds) **Bit 1:** Disable Host Reset Timer **Bit 2:** Disable CPU_RESET_DONE timeout **Bit 3:** Reserved **Bit 4:** Disable Intel® ME Power Gating **Bit 5:** Reserved **Bit 6:** Secure Boot debug hook. Used to shorten wait time before ENF shutdown. **Bit 7:** Force real FPFs on preproduction (default is to use flash) **Bit 8:** Secure Boot debug hook. Used to reduce S3 or FFS optimization tries. **Bit 9:** Reserved **Bit 10:** Override power package to always enter M3. **Note:** Certain options do not work when the descriptor is locked.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
	Debug Override Production Silicon - Allows the OEM to control FW features to assist with production platform debugging. **Bit 0:** Extend DRAM_INIT_DONE timeout to 30 minutes (default timeout 15 seconds) **Bit 1:** Disable Host Reset Timer **Bit 2:** Disable CPU_RESET_DONE timeout **Note:** Certain options do not work when the descriptor is locked.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000000 0x00000000
	Enable Intel® ME Reset Capture on CLR_RST# **Values: Yes/No -** This setting configures Intel® ME behavior when it resets during CL_RST#1. **Note:** The recommended default for this setting is "No".	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Firmware ROM Bypass **Values: Yes/No** - This setting enables / disables firmware ROM bypass. **Note:** This setting only has affect when the firmware being used has ROM Bypass code present.	SKL-Y SKL-U SKL-H SKL-S	No No No No

Click on Debug in the left tabs menu> Direct Connection Interface Configuration is expanded by default:

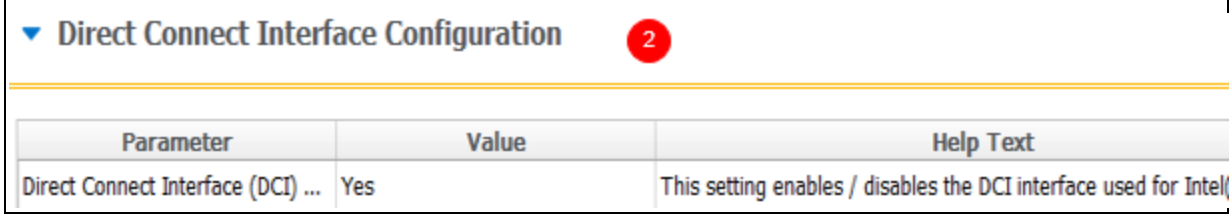
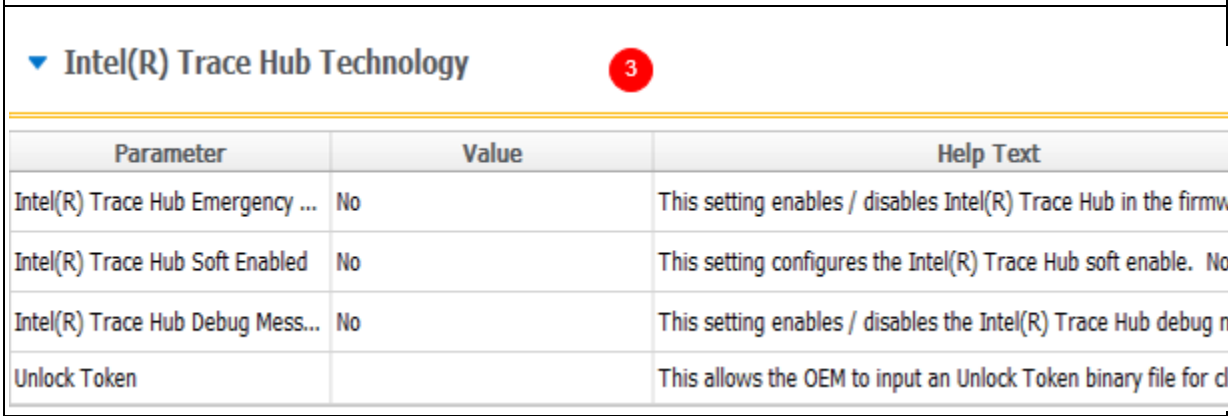


Table 2-15. Intel® FIT - Debug (Sheet 2 of 3)

#	Parameter	Platform	Settings
2	**Debug - Direct Connection Interface Configuration**		
	Direct Connect Interface (DCI) Enabled **Values: Yes / No** - This setting enables / disables the DCI interface used for Intel® Trace Hub debugging.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
Click on Debug in the left tabs menu> Intel® Trace Hub Technology is expanded by default:			



#	Parameter	Platform	Settings
3	**Debug - Intel® Trace Hub Technology**		
	Intel® Trace Hub Emergency Mode Enabled **Values: Yes / No** - This setting enable / disables Intel® Trace Hub in the firmware base image.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Intel® Trace Hub Soft Enabled **Values: Yes / No** - This setting configures the Intel® Trace Hub soft enable. **Note:** When enabling this setting you also need to enable Intel® Trace Hub Debug Messages setting for proper operation.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Intel® Trace Hub Debug Message Enabled **Values: Yes / No** - This setting enables/disables the Intel® Trace Hub debug messages. **Note:** When enabling this setting you also need to enable Intel® Trace Hub Soft Enable setting for proper operation.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Unlock Token This allows the OEM to input an Unlock Token binary file for closed chassis debug.		
Click on Debug in the left tabs menu> Intel® IDLM is expanded by default:			

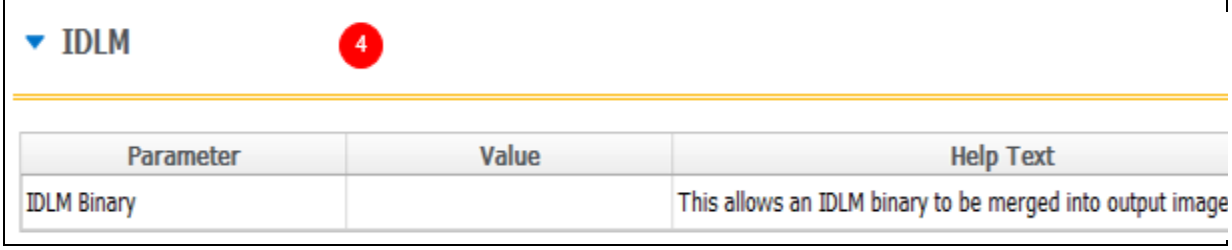


Table 2-15. Intel® FIT - Debug (Sheet 3 of 3)

#	Parameter	Platform	Settings
4	**Debug - Intel® IDLM**		
	Intel® IDLM This allows an IDLM binary to be merged into output image built by Intel® FIT.		

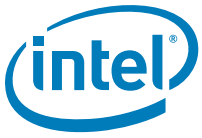


Table 2-16. Intel® FIT - CPU Straps (Sheet 1 of 3)

Click on CPU Straps in the left tabs menu> CPU Straps are expanded by default:

▼ CPU Straps 1

Parameter	Value	Help Text
Disable Hyperthreading	No	This setting control enabling / disabling of Hyper threading. Note: This strap is in
Number of Active Cores	All	This setting controls the number of active processor cores. Note: This strap is int
BIST Initialization	No	This setting determines if BIST will be run at platform reset after BIOS requested
Flex Ratio	0x0	This setting controls the maximum processor non-turbo ratio. Note: This strap is
Processor Boot Max Frequency	Yes	This setting determines if the processor will operate at maximum frequency at p
JTAG Power Disable	No - No JTAG Power on C10 an...	This setting determines if JTAG power will be maintained on C10 or lower power
SA Power Plane Topology	0x2	This setting determines the SA power plane topology. See Processor EDS for det
SA VR Type	SVID	This setting determines the SA core domain VR type. See Processor EDS for deta
IA Power Plane Topology	0x0	This setting determines the IA power plane topology. See Processor EDS for deta
IA Power Plane VR	SVID	This setting determines the IA core domain VR type. See Processor EDS for deta
Ring Power Plane Topology	0x0	This setting determines the Ring power plane topology. See Processor EDS for d
Ring VR Type	SVID	This setting determines the Ring domain VR type. See Processor EDS for details.
GT_US Power Plane Topology	0x1	This setting determines the GT Unslice power plane topology. See Processor EDS
GT_US VR Type	SVID	This setting determines the GT Unslice domain VR type. See Processor EDS for d
GT_S Power Plane Topology	0x1	This setting determines the GT slice power plane topology. See Processor EDS fo
GT_S VR Type	SVID	This setting determines the GT slice domain VR type. See Processor EDS for deta
SVID Presence	SVID Present	This setting determine if SVID rails are present on the platform. See Processor E
Platform IMON Disable	0x0	This strap should be left at the recommended default setting.
eOPIO Power Plane Topology	0x0	This setting determines the eOPIO power plane topology. See Processor EDS for
eOPIO VR Type	Fixed VR	This setting determines the eOPIO domain VR type. See Processor EDS for detail
EDRAM Power Plane Topology	0x0	This setting determines the EDRAM power plane topology. See Processor EDS fo
EDRAM VR Type	Fixed VR	This setting determines the EDRAM domain VR type. See Processor EDS for deta
SE Key Mode	0	Note: This strap should be left at the recommended default setting.

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Table 2-16. Intel® FIT - CPU Straps (Sheet 2 of 3)

#	Parameter	Platform	Settings
1	**CPU Straps - CPU Straps**		
	Disable Hyperthreading **Values: Yes/No** This setting controls enabling or disabling of Hyper threading. **Note:** This strap is intended for debugging purposes only. See BIOS Spec for more details on enabling / disabling Hyperthreading.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Number of Active Cores **Values: All, 1, 2, 3, 4** This setting controls the number of active processor cores. **Note:** This strap is intended for debugging purposes only. See BIOS Spec for more details on enabling or disabling processor cores.	SKL-Y SKL-U SKL-H SKL-S	All All All All
	BIST Initialization **Values: Yes/No** This setting determines if BIST will be run at platform reset after BIOS requested actions. **Note:** This strap is intended for debugging purposes only.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	Flex Ratio This setting controls the maximum processor non-turbo ratio. **Note:** This strap is intended for debugging purposes only. See BIOS Spec for more details on maximum processor non-turbo ratio configuration.	SKL-Y SKL-U SKL-H SKL-S	0x0 0x0 0x0 0x0
	Processor Boot Max Frequency **Values: Yes/No** This setting determines if the processor will operate at maximum frequency at power-on and boot. **Note:** This strap is intended for debugging purposes only.	SKL-Y SKL-U SKL-H SKL-S	Yes Yes Yes Yes
	JTAG Power Disable **Values: Yes - JTAG Power on C10 and Lower/No - No Power on C10 and Lower** This setting determines if JTAG power will be maintained on C10 or lower power states. **Note:** This strap is intended for debugging purposes only.	SKL-Y SKL-U SKL-H SKL-S	No No No No
	SA Power Plane Topology This setting determines the SA power plane topology. See Processor EDS for details. **Note:** This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0x2 0x2 0x2 0x2
	SA VR Type **Value: SVID/Fixed VR** This setting determines the SA core domain VR type. See Processor EDS for details.	SKL-Y SKL-U SKL-H SKL-S	SVID SVID SVID Fixed VR
	IA Power Plane Topology This setting determines the IA power plane topology. See Processor EDS for details. **Note:** This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0x0 0x0 0x0 0x0
	IA Power Plane VR **Value: SVID/Fixed VR** This setting determines the IA core domain VR type. See Processor EDS for details.	SKL-Y SKL-U SKL-H SKL-S	SVID SVID SVID SVID
	Ring Power Plane Topology This setting determines the Ring power plane topology. See Processor EDS for details. **Note:** This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0x0 0x0 0x0 0x0
	Ring VR Type **Value: SVID/Fixed VR** This setting determines the Ring domain VR type. See Processor EDS for details.	SKL-Y SKL-U SKL-H SKL-S	SVID SVID SVID SVID

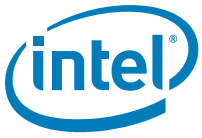
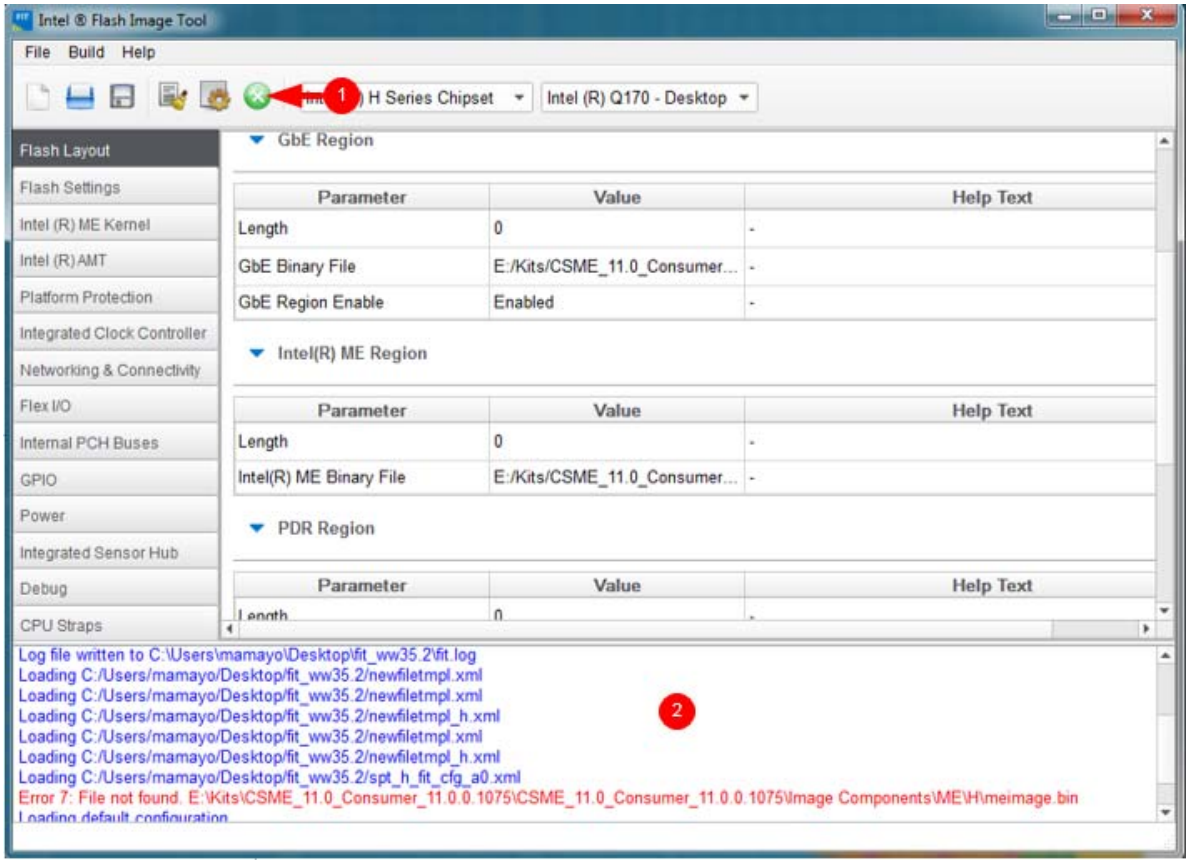


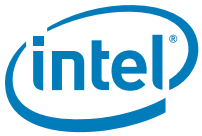
Table 2-16. Intel® FIT - CPU Straps (Sheet 3 of 3)

#	Parameter	Platform	Settings
	GT_US Power Plane Topology This setting determines the GT Unslice power plane topology. See Processor EDS for details. **Note:** This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0x1 0x1 0x1 0x1
	GT_US VR Type **Value: SVID/Fixed VR** This setting determines the GT Unslice domain VR type. See Processor EDS for details.	SKL-Y SKL-U SKL-H SKL-S	SVID SVID SVID SVID
	GT_S Power Plane Topology This setting determines the GT slice power plane topology. See Processor EDS for details. **Note:** This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0x1 0x3 0x3 0x3
	GT_SVR Type **Value: SVID/Fixed VR** This setting determines the GT slice domain VR type. See Processor EDS for details.	SKL-Y SKL-U SKL-H SKL-S	SVID SVID SVID SVID
	SVID Presence **Value: SVID Present/SVID Not Present** This setting determines if SVID rails are present on the platform. See Processor EDS for details.	SKL-Y SKL-U SKL-H SKL-S	SVID Present SVID Present SVID Present SVID Present
	Platform IMON Disable This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0x0 0x0 0x1 0x1
	eOPIO Power Plane Topology This setting determines the eOPIO power plane topology. See Processor EDS for details. **Note:** This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000005 0x00000005
	eOPIO VR Type **Value: SVID/Fixed VR** This setting determines the eOPIO domain VR type. See Processor EDS for details.	SKL-Y SKL-U SKL-H SKL-S	Fixed VR Fixed VR Fixed VR Fixed VR
	EDRAM Power Plane Topology This setting determines the EDRAM power plane topology. See Processor EDS for details. **Note:** This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0x00000000 0x00000000 0x00000004 0x00000004
	EDRAM VR Type **Value: SVID/Fixed VR** This setting determines the EDRAM domain VR type. See Processor EDS for details.	SKL-Y SKL-U SKL-H SKL-S	Fixed VR Fixed VR Fixed VR Fixed VR
	SE Key Mode **Note:** This strap should be left at the recommended default setting.	SKL-Y SKL-U SKL-H SKL-S	0 0 0 0

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Table 2-17. Intel® FIT - Build Image

#	Parameter	CRB	Values
			
1	**Green Build button**		Can also select CTRL+B, or Build> Build Image from the menu bar along the top of the screen
2	**Console shows status of build and path where saved**		



3 Programming SPI Flash Devices and Checking Firmware Status

Now that the Flash image file has been created, it can be programmed into the SPI Flash device(s) of the target machine. For platforms that don't boot, a Flash Chip Programmer will be required. For platforms that can boot to DOS or Windows*, the Intel® FPT can be used.

3.1 Flash Burner/Programmer

The specific use of a Flash burner/programmer is beyond the scope of this document. Here are some general steps that may be followed:

1. Navigate to your **Output Directory** (as specified in Table 2-2) where your generated SPI Flash image(s) are saved. It is assumed that this image file is named **outimage.bin**.

   If two total SPI Flash devices were specified during the build process, then additional image files will be saved, one for each SPI Flash device. These files are assumed to be named **outimage(1).bin** and **outimage(2).bin**.
2. Utilize a Flash burner/programmer to program the image(s). For multiple SPI Flash devices, the images are numbered sequentially to correspond to the first and second SPI Flash device accordingly.

3.1.1 In-Circuit SPI Flash Programming for CRB

Mobile CRBs have the SPI Flash devices soldered down. As a result, to program the SPI Flash for mobile CRBs, follow these steps:

1. Leave CRB powered on.
2. Connect Flash Programmer (such as DediProg SF600) header to connector **J3F3** which is labelled **"SPI TPM"**. Make sure to line up pin 1 on the header.
3. Program the first image [outimage(1).bin] to the CRB.
4. In Dediprog software, select application memory chip 2 button and load second image if created.
5. Program the second image [outimage(2).bin] to the CRB if created.
6. Once programming is complete, disconnect the Flash Programmer header. Power off and unplug CRB. Remove cell coin battery, wait approximately 10 seconds. Replace cell coin battery, plug CRB back in and power on.

3.2 Flash Programming Tool (Intel® FPT)

Intel® FPT can be used to substitute for a Flash burner/programmer, provided the system is capable of booting to a DOS or Windows* OS.

Note: Intel® FPT will automatically disable the Intel® ME or EFI prior to flashing the image to the platform.

Intel® FPT DOS Version

The DOS versions supported by Intel® FPT are: DOS, Free DOS, and DRMK DOS. Use the following steps to program the SPI Flash devices,

1. Copy all the files in the "(root)\Tools\System Tools\Flash Programming Tool\DOS" directory to the root directory of a bootable USB key.
2. Navigate to your **Output Directory** (as specified in Table 2-2) where your generated SPI Flash image(s) are saved. It is assumed that this image file is named **outimage.bin**. Copy this image file to the root directory of the USB key.
3. Boot the target system to DOS and change to the root directory of the bootable USB key. At the DOS prompt type:

```
fpt.exe -i
```

   The system should respond with the number of SPI Flash devices available. For example:

```
--- Flash Devices Found ---
W25Q64BV ID:0xEF4017 Size: 8192KB (65536Kb)
W25Q64BV ID:0xEF4017 Size: 8192KB (65536Kb)
```

   Note: If the SPI Flash device does not currently contain a descriptor it may report only a single device.

4. Program the SPI Flash image to the Flash device(s) by issuing the following command at the prompt:

```
fpt.exe -f outimage.bin
```

   If the programming was successful, then the following message will be shown.

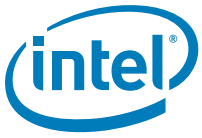
```
FPT Operation Passed
```

   If the programming was **NOT** successful, then repeat this step to try again. If programming problems persist, then check the SPI Flash devices and platform hardware.

5. Execute a platform global reset using Intel® FPT -greset. Next go to Section 3.3 to check the Intel® ME Firmware status.

3.2.1 Intel® FPT Windows* Version

The Windows* OS versions supported by Intel® FPT are: Windows* PE 64, Windows* 7, Windows* 8/8.1. There are two versions of Intel® FPT for Windows*: a 32-bit version and a 64-bit version. Most Windows* OS, Windows* 7 (32-bit or 64-bit), Windows* 8/8.1 (32-bit or 64-bit) can use Windows* version of Intel® FPT. However, Windows* OS which do not support 32 bit compatible mode (Win PE 64-bit) **must use** Intel® FPT Windows* 64-bit version due to compatibility issues.



Use the following steps to program the SPI Flash devices,

1. Navigate to your **Output Directory** (as specified in Table 2-2) where your generated SPI Flash image(s) are saved. It is assumed that this image file is named **outimage.bin**. Copy this image file to Intel® FPT directory located at "(root)\Tools\System Tools\Flash Programming Tool\Windows".
2. Boot the target system to Windows* and open a Command Prompt window. In this window, change to the Intel® FPT directory and at the prompt type:

```
fptw.exe -i
```

   The system should respond with the number of SPI Flash devices available. For example:

```
--- Flash Devices Found ---
W25Q64BV ID:0xEF4017 Size: 8192KB (65536Kb)
W25Q64BV ID:0xEF4017 Size: 8192KB (65536Kb)
```

   Note: If the SPI Flash device does not currently contain a descriptor it may report only a single device.

3. Program the SPI Flash image to the Flash device(s) by issuing the following command at the prompt:

```
fptw.exe -f outimage.bin
```

   If the programming was successful, then the following message will be shown.

```
FPT Operation Passed
```

   If the programming was **NOT** successful, then repeat this step to try again. If programming problems persist, then check the SPI Flash devices and platform hardware.

4. Use fptw.exe -greset to perform a G3 power cycle. Next go to Section 3.3 to check the Intel® ME Firmware status.

3.3 Checking Intel® ME Firmware Status

Use the following steps to check the platform health and Intel® ME FW status,

1. Copy the file **MEInfo.exe** in the "(root)\Tools\System Tools\MEInfo\DOS" directory to the root directory of a bootable USB key.
2. Boot the target system and use F2 or Del to enter the BIOS setup menu. Load default values for BIOS (on Intel® CRBs press F3 to load default values). Save and reboot (on Intel® CRBs press F4 and select Yes).
3. Boot the target system to DOS and change to the root directory of the bootable USB key. At the DOS prompt type:

```
MEInfo.exe -fwsts
```

The system should respond with a message similar to below.

```
Intel® MEInfo Version: 11.0.0.xxxx

Copyright(C) 2005 - 2014, Intel Corporation. All rights reserved.

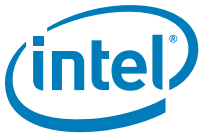
FW Status Register1: 0x1E000255
FW Status Register2: 0x60002306
FW Status Register3: 0x00000300
FW Status Register4: 0x00004001
FW Status Register5: 0x00000101
FW Status Register6: 0x03C00FC9

  Current State: Normal
  ManufacturingMode: Enabled
  FlashPartition:                  Valid
  OperationalState:                        M0 with UMA
  InitComplete:              Complete
  BUPLoadState:                Success
  ErrorCode:                No Error
  ModeOfOperation:                      Normal
  Phase:                  HOSTCOMM Module
  ICC:                       Valid OEM data, ICC programmed
  SPI Flash Log:                              Not Present
  ME File System Corrupted:                                 No
  FPF and ME Config Status:                                 Not committed
```

As in the above example if there are NO errors shown, then

- your platform's health is good
- Intel® ME FW has successfully initialized
- Intel® ME FW is operating normally

Note: This section is only intended to show how to use the MEInfo.exe tool for checking firmware status. For full usage and capabilities of the MEInfo.exe tool, please see the System Tools User Guide.



3.4 Common Bring Up Issues and Troubleshooting Table

Table 3-1. Common Bring Up Issues and Troubleshooting Table

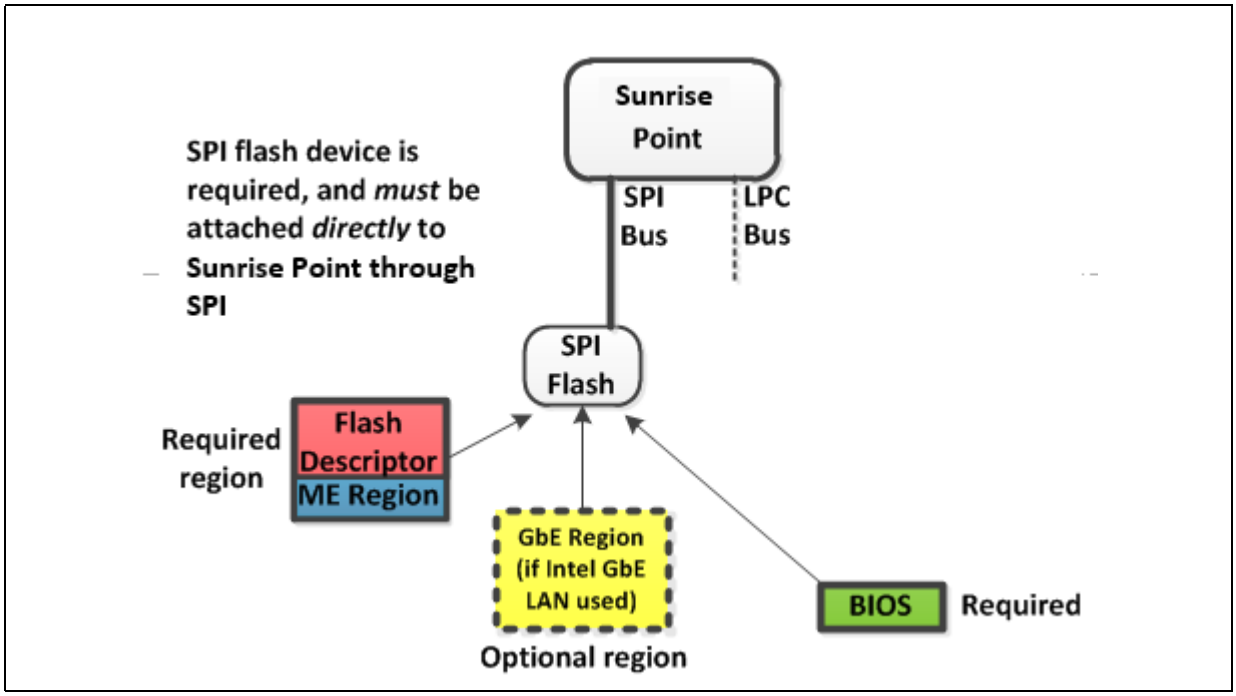
Problem / Issue	Solution / Workaround
System does not boot to DOS	By default, the system will boot to EFI Shell. To boot to DOS, 1. Enter BIOS menu, then go to the 'Boot' screen 2. Change 'Boot Option #1' to be your USB key (ensure USB key is formatted to be DOS bootable) 3. Press 'F4' to save settings and reboot
Hear 3 beeps when platform powers on	Possible device is disconnected or device not found, check • platform power and MCP fan power connectors • DIMM memory modules (if applicable for memory down modules • USB devices (keyboard, mouse, USB key) may be plugged into inactive USB port • missing/incorrect jumpers • missing or poorly socketed MCP
No display on monitor	Ensure Corporate FW SKU supports integrated graphics. Try external graphics card.
USB device not detected or does not work	USB device may be plugged into inactive USB port
System does not boot (Post Code 00)	Incorrect Flash image – possible reasons: • wrong FW selected during Flash image build process • wrong Flash size selected Re-build image with correct settings and re-flash using Flash burner.

§ §

A Appendix — Flash Configurations

This chapter covers only the basic information needed for clock control parameter programming. For a more detailed treatment of Mainstream - Mobile Family clocks, see Intel® *Skylake PCH-LP Clocks* and *Intel® Management Engine — Platform Compliancy Guide for ME Hardware*.

Figure A-1. Configuration "A" — Desktop / Server / Workstation or Mobile



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Figure A-2. Configuration "B" — Mobile Only

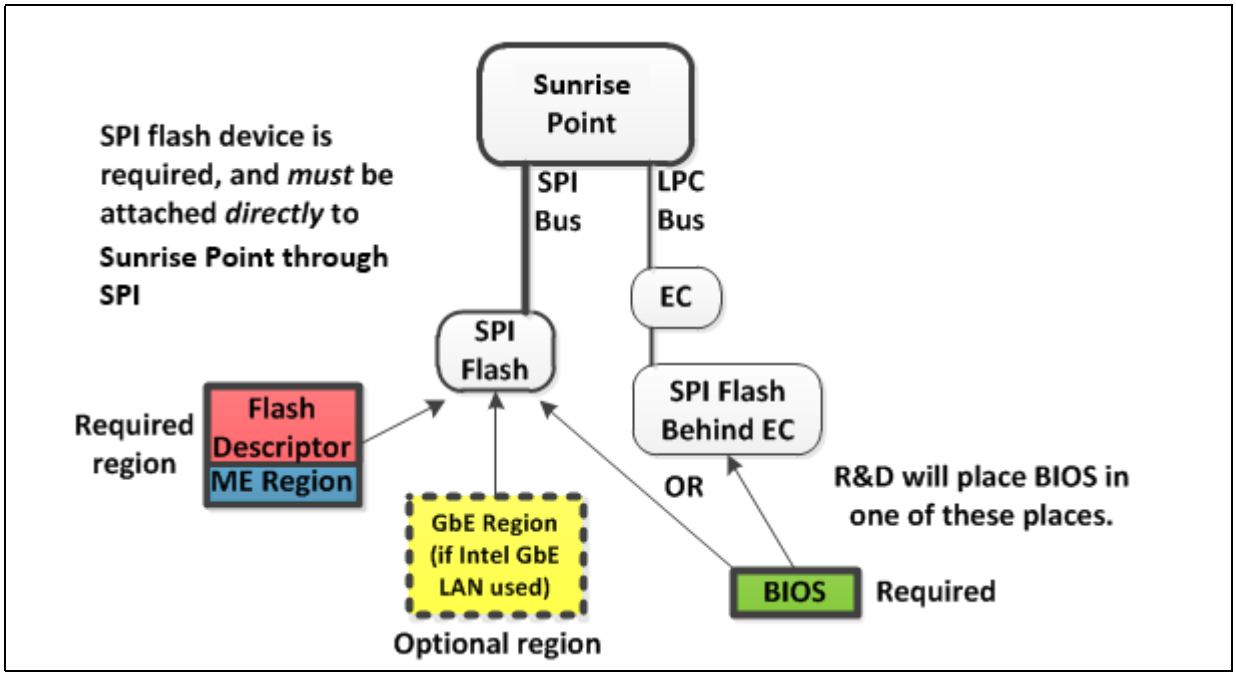
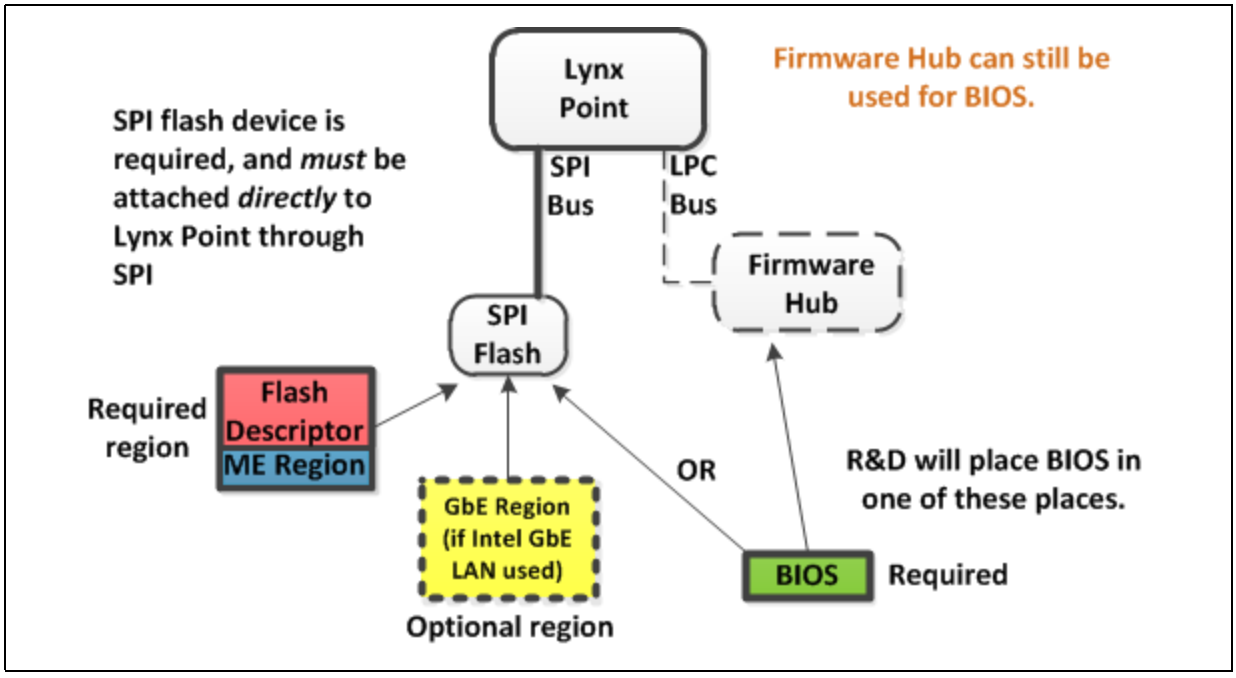
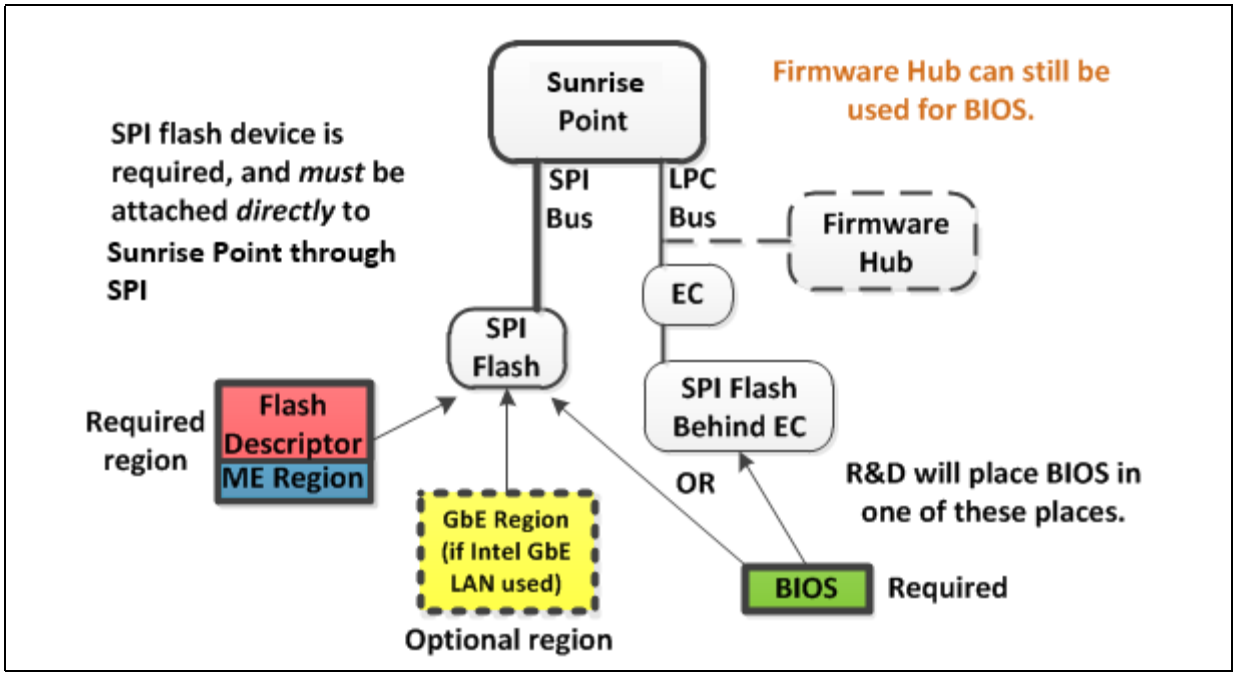


Figure A-3. Configuration "C" — Desktop / Server / Workstation Only

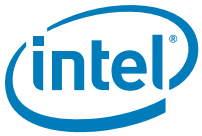


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Figure A-4. Configuration “D” — Mobile Only



§ §



B Appendix — Intel® ICCS SKU Support Matrix

The following tables describes ICC features supported for specific PCH SKU, clock range (maximum and minimum), spread mode supported by Skylake Platform SKUs (SPT-H and SPT-LP PCH).

Note: Please refer to Skylake-LP/H Platform Controller Hub (PCH) External Design Specification (EDS) for details about Skylake Platform I/O - Chipset Clock Architecture.

For table B.1 - Min = Clock Div Max (minimum allowed frequency) and Max = Clock Div Min (maximum allowed frequency)

B.1 Intel® ICCS SKU Matrix - SPT-LP

Note: ICC SKU is divided into 2 categories: Basic and Enhanced. Mark "x" indicates category supported by PCH SKU.

Table B-1. Intel® ICCS SKU Matrix - SPT-LP

PCH SKU	Basic	Enhanced
Premium Y		**x**
Premium U		**x**
Base U		**x**
Features Supported	Standard Clock Configuration	Standard Clock Configuration Adaptive Clock Configuration
Pre-Defined ICC profile supported	Standard	Standard Adaptive
Clock Range Supported	[Min-Max]=100 MHz.	BCLK [Min-Max] = 98 - 100 MHz.
SSC Supported	Down SSC: 0 - 0.5%	Down SSC: 0 - 0.5%

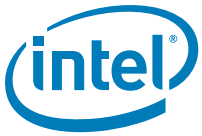
B.2 Intel® ICCS SKU Matrix - SPT-H

Note: ICC SKU is divided into 3 categories: Basic ,Enhanced and Extreme. Mark "x" indicates category supported by PCH SKU.

Table B-2. Intel® ICCS SKU Matrix - SPT-H

PCH SKU	Basic	Enhanced	Extreme
Q170		x	
Q150		x	
B150		x	
H170		x	
Z170			x
H110		x	
QM170			x
HM170			x
CM236			x
Features Supported	Standard clock configuration	Standard clock configuration Adaptive clock configuration	Standard clock configuration Adaptive clock configuration BCLK Overclocking clock configuration
Pre-Defined ICC profile supported	Standard	Standard Adaptive	Standard Adaptive OverClocking OverclockingPlus
Clock Range Supported	[Min-Max]=100 MHz.	BCLK [Min-Max] = 98 - 100 MHz.	BCLK Over clocking [Min-Max] = 99.5 -170 MHz * BCLK Over clocking Plus [Min-Max] = 99.5 -341 MHz*
SSC Supported	Down SSC: 0 - 0.5%	Down SSC: 0 - 0.5%	BCLK Over clocking Down SSC : 0 - 0.5% BCLK Over clocking Plus Down SSC : 0 - 0.2%

*BCLK Overclocking ranges mentioned here are ranges supported by The Intel® ME FW, please make sure to choose range based on platform/HW configuration.



C Appendix — Boot Guard Configuration

C.1 Boot Guard Profiles

The following table describes the profiles available for Boot Guard Configuration.

Table C-1. Profile Description

Index	Profile Name	F	V	M	ENF	PBE	Description
0	**Boot Guard Profile - No_FVME**	0	0	0	00	0	This configuration will invoke Boot Guard during boot with neither Verification nor Measurement. For platforms with all the required Boot Guard components but do not wish to enable Boot Guard boot block verification protection.
1	**Boot Guard VE**	0	1	0	01	1	When Verification is desired but if verification fails the platform will continue to boot with the unverified IBB for a short period, to allow remediation.
2	**Boot Guard VME**	0	1	1	01	1	When Verification and Measured are desired and the asset protection is provided by both TPM protection and a timed remediation period.
3	**Boot Guard VM**	0	1	1	00	1	When Verification and Measured are desired and the asset protection is provided by TPM protection.
4	**Boot Guard FVE**	1	1	0	11	1	Strict Verification enforcement.
5	**Boot Guard FVME**	1	1	1	11	1	Strict Verification and Measured enforcement. Prevents unverified IBB from running.

C.2 Enforcement Policies

Table C-2. Enforcement Policy Description

Error Enforcement Policy (ENF)	Enforcement Mode Name	Description
0	**Unrestricted Mode**	Infinite time before shutdown – don't shutdown the platform, let everything run normally.
1	**Remediation Mode**	**30 minutes** before shutdown – enough time to remediate the system, e.g. update BIOS or other data on flash via host tools.
2	**Reserved**	
3	**Restricted Mode**	**0 minutes** before shutdown – instant shutdown policy.

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C.3 OEM Profile Parameters

Table C-3. Profile Parameters Description

Parameter	Description	Settings
Force Boot Guard ACM Enabled (F)	Force Boot Guard Boot determines if the platform starts the Force Boot Guard Boot timer. If it successfully starts it indicates success. When the Force Boot Guard timer stops, it starts the Protect Bios Environment timer, if indicated by the boot policy restrictions. Anchor ACM then jumps to the Initial Boot Block(IBB) with the Force Boot Guard Boot time stopped and the Protect BIOS enable timer running.	**false** - Allow the CPU to jump to the legacy reset vector if the Boot Guard Module cannot be successfully loaded. (default) **true -** Force the Boot Guard ACM to execute.
Verified Boot Enabled (V)	Boot Guard cryptographically verifies the platform Initial Boot Block (IBB) using the boot policy key. On successful verification, Boot Guard executes Initial Boot Block (IBB) using the boot policy key. If the verification fails, Anchor signals or enters Remediation.	**false** - Platform does not perform verified boot (default) **true** - Platform performs verified boot
Measured Boot Enabled (M)	Boot Guard measures the Initial Boot Block (IBB) into the TPM. Boot Guard perform no verification that the IBB is correct or from the platform manufacturer. The Slylake implementation of Boot Guard will support measurements into TPM or Intel's Platform Trust Technology.	**false** - Platform does not perform measured boot (default) **true** - Platform performs measured boot
Protect Bios Environment Enabled (PBE)	Platform manufacturer may want Initial boot block to be protected between verification/ measurement and execution from attacks on buses and non-CPU components. Boot Guard accomplishes this by allowing the initial boot block to be verified and executed in LLC in NEM if PBE is enabled.	**false** - Take no actions to control the environment during execution of the BIOS components (default) **true** - Takes actions to control the environment during the execution of the BIOS components.
Error Enforcement Policy (ENF)	Boot Guard invokes the Enforcement Policy when a fatal error is encountered. The action taken by ENF is determined by the OEM set persistent policies. Like, • Allowing platform to continue to boot • Immediate Shutdown • Shutdown with Timeout intervals When the ENF logic is invoked, PTT or TPM also disconnects.	See Section C-2 for details.

D Appendix — Intel® Platform Trust Technology

D.1 Intel® Platform Trust Technology

The following table describes the platform configurations supported by Intel® Platform Trust Technology.

Note: Intel® Platform Trust Technology does not support the full TPM functionality requirements and should not be used for Intel® vPro™ based platforms.

Table D-1. Intel® Platform Trust Technology Configuration table

Configuration	Platform Protection> Intel® PTT Configuration Intel® PTT initial power up state	Platform Protection> Intel® PTT Configuration Intel® PTT Supported	Platform Protection> Intel® PTT Configuration Intel® PTT Supported [FPF]	Description
Intel® PTT Permanently Disabled in HW via FPF	**Disabled**	**No**	**No**	After the End of Manufacturing command, this setting will permanently set into the FPFs contained in the MCP. If disabled, the specific MCP can never be enabled for Intel® PTT.
Intel® PTT Permanently Disabled in base firmware image	**Disabled**	**No**	**Yes**	This setting allows Intel® PTT to be set to disabled without disabling the MCP FPFs. This is the recommended option to permanently disable Intel® PTT on a platform.
Intel® PTT Ship State Disabled in base firmware image	**Disabled**	**Yes**	**Yes**	Intel® PTT initially shipped in disabled mode, can be enabled by BIOS command.
Intel® PTT Enabled	**Enabled**	**Yes**	**Yes**	This is the recommended option to enable Intel® PTT on a platform.

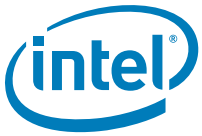
E Appendix — Settings for RVP CRBs (B)

The following table describes the configuration settings required for RVP CRBs in the Intel® FIT tool. Please see SPI Programming Guide for additional details.

Table E-1. Skylake-LP RVP Board Settings - B Step

CRB Board	Setting Name	Intel® FIT Visible	Offset	Value
RVP5	SATA / PCIe GP Select for Port 0	No	0x168 [1:0]	0x3
	SATA / PCIe GP Select for Port 2	No	0x168 [5:4]	0x3
	USB3 / PCIe Combo Port 0 Strap	No	0x16E [1:0]	0x0
	USB3 / PCIe Combo Port 1 Strap	No	0x16E [3:2]	0x0
	GbE PCIe Port Select	Yes	0x17C [5:3]	PORT4
	SATA / PCIe Combo Port 0 Strap	Yes	0x17D [1:0]	GPIO
	SATA / PCIe Combo Port 3 Strap	Yes	0x180 [1:0]	GPIO
	USB3 / PCIe Combo Port 0	Yes	0x182 [1:0]	USB3
	USB3 / PCIe Combo Port 1	Yes	0x182 [3:2]	USB3
	SATA / PCIe Select for Port 0	No	0x18C [1:0]	0x3
	SATA / PCIe Select for Port 1	No	0x18C [3:2]	0x3
	PCIe Controller 1 (Port 1-4)	Yes	0x19D [4:3]	4x1
	PCIe Controller 2 (Port 5-8)	Yes	0x1A5 [4:3]	1x2, 2x1
	PCIe Controller 3 (Port 9-12)	Yes	0x1AD [4:3]	1x4
	PCIe Controller 3 Lane Reversal Enabled	Yes	0x1AD [2]	Yes
	XHCI Port 4 Ownership	Yes	0x1B8 [4]	XHCI
	XHCI Port 5 Ownership	Yes	0x1B8 [5]	XHCI
RVP7	SATA / PCIe GP Select for Port 0	No	0x168 [1:0]	0x0
	SATA / PCIe GP Select for Port 2	No	0x168 [5:4]	0x3
	USB3 / PCIe Combo Port 0 Strap	No	0x16E [1:0]	0x0
	USB3 / PCIe Combo Port 1 Strap	No	0x16E [3:2]	0x0
	GbE PCIe Port Select	Yes	0x17C [5:3]	PORT4
	SATA / PCIe Combo Port 1 Strap	Yes	0x17D [3:2]	SATA
	SATA / PCIe Combo Port 3 Strap	Yes	0x180 [1:0]	GPIO
	USB3 / PCIe Combo Port 0	Yes	0x182 [1:0]	USB3
	USB3 / PCIe Combo Port 1	Yes	0x182 [3:2]	USB3
	SATA / PCIe Select for Port 1	No	0x18C [1:0]	0x0
	SATA / PCIe Select for Port 2	No	0x18C [5:4]	0x3
	PCIe Controller 1 (Port 1-4)	Yes	0x19D [4:3]	4x1
	PCIe Controller 3 (Port 9-12)	Yes	0x1AD [4:3]	1x4
	PCIe Controller 3 Lane Reversal Enabled	Yes	0x1AD [2]	Yes
	XHCI Port 4 Ownership	Yes	0x1B8 [4]	XHCI
	XHCI Port 5 Ownership	Yes	0x1B8 [5]	XHCI

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Note: The Intel® FIT default settings for Skylake-LP are based on the RVP3 CRB.

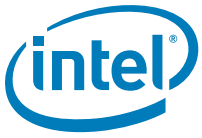
Table E-2. Skylake-H RVP Board Settings - B Step

CRB Board	Intel® FIT Setting Name	Intel® FIT Visible	Offset	Value
	SATA / PCIe GP Select for Port 0	No	0x1AC[1:0]	0x3
	SATA / PCIe GP Select for Port 1	No	0x1AC [3:2]	0x3
	SATA / PCIe GP Select for Port 2	No	0x1AC [5:4]	0x0
	SATA / PCIe GP Select for Port 3	No	0x1AC [7:6]	0x0
	SATA / PCIe GP Select for Port 4	No	0x1AD[1:0]	0x3
	SATA /PCIe Combo Port 2	Yes	0x1C1 [5:4]	GPIO
	SATA /PCIe Combo Port 3	Yes	0x1C4 [1:0]	GPIO
	SATA /PCIe Combo Port 4	Yes	0x1C4 [3:2]	SATA
	SATA /PCIe Combo Port 5	Yes	0x1C4 [5:4]	SATA
	SATA /PCIe Combo Port 6	Yes	0x1C4 [7:6]	GPIO
	Polarity Select SATA / PCIe Combo Port 2	Yes	0x1C8 [2]	SATA
	Polarity Select SATA / PCIe Combo Port 3	Yes	0x1C8 [3]	SATA
RVP8	**Polarity Select SATA / PCIe Combo Port 4**	Yes	0x1C8 [4]	PCIe
	Polarity Select SATA / PCIe Combo Port 5	Yes	0x1C8 [5]	PCIe
	Polarity Select SATA / PCIe Combo Port 6	Yes	0x1C8 [6]	SATA
	SATA / PCIe Select for Port 0	No	0x1D0 [1:0]	0x3
	SATA / PCIe Select for Port 1	No	0x1D0 [3:2]	0x3
	SATA / PCIe Select for Port 2	No	0x1D0 [5:4]	0x0
	SATA / PCIe Select for Port 3	No	0x1D0 [7:6]	0x0
	SATA / PCIe GPIO Polarity Port 0	No	0x1D2 [0]	0x1
	SATA / PCIe GPIO Polarity Port 1	No	0x1D2 [1]	0x1
	SATA / PCIe GPIO Polarity Port 2	No	0x1D2 [2]	0x0
	SATA / PCIe GPIO Polarity Port 3	No	0x1D2 [3]	0x0
	SATA / PCIe GPIO Polarity Port 4	No	0x1D2 [4]	0x1
	PCIe Controller 4 (Port 13-16)	Yes	0x1F9 [4:3]	1x2, 2x1
RVP9	**DMI Lane Reversal**	Yes	0x25E [5]	Yes
RVP11	**SATA / PCIe GP Select for Port 0**	No	0x1AC[1:0]	0x0
	SATA / PCIe GP Select for Port 1	No	0x1AC [3:2]	0x0
	SATA / PCIe GP Select for Port 2	No	0x1AC [5:4]	0x3
	SATA / PCIe GP Select for Port 3	No	0x1AC [7:6]	0x3
	USB3 / PCIe Combo Port 3 Strap	No	0x1B2 [7:6]	0x1
	SATA /PCIe Combo Port 2	Yes	0x1C1 [5:4]	GPIO
	SATA /PCIe Combo Port 3	Yes	0x1C4 [1:0]	GPIO
	SATA /PCIe Combo Port 4	Yes	0x1C4 [3:2]	SATA
	SATA /PCIe Combo Port 5	Yes	0x1C4 [5:4]	SATA
	USB3 / PCIe Combo Port 3	Yes	0x1C6 [7:6]	USB3

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CRB Board	Intel® FIT Setting Name	Intel® FIT Visible	Offset	Value
	Polarity Select SATA / PCIe Combo Port 2	Yes	0x1C8 [2]	SATA
	Polarity Select SATA / PCIe Combo Port 3	Yes	0x1C8 [3]	SATA
	Polarity Select SATA / PCIe Combo Port 4	Yes	0x1C8 [4]	PCIe
	Polarity Select SATA / PCIe Combo Port 5	Yes	0x1C8 [5]	PCIe
	SATA / PCIe Select for Port 0	No	0x1D0 [1:0]	0x3
	SATA / PCIe Select for Port 1	No	0x1D0 [3:2]	0x3
	SATA / PCIe Select for Port 2	No	0x1D0 [5:4]	0x0
	SATA / PCIe Select for Port 3	No	0x1D0 [7:6]	0x0
	SATA / PCIe GPIO Polarity Port 0	No	0x1D2 [0]	0x1
	SATA / PCIe GPIO Polarity Port 1	No	0x1D2 [1]	0x1
	SATA / PCIe GPIO Polarity Port 2	No	0x1D2 [2]	0x0
	SATA / PCIe GPIO Polarity Port 3	No	0x1D2 [3]	0x0
	XHCI Port 10 Ownership	Yes	0x20D [1]	XHCI

Note: The Intel® FIT default strap settings for Skylake-H are based on the RVP10 CRB.



F Appendix — Integrated Sensor Hub (ISH) Public Key Settings

The following table describes the configuration matrix required for ISH configuration for the Intel® FIT tool. Please see System Tools User Guide within ME kit, Manufacturing Test with Intel® Management Engine (Intel® ME) Firmware 11 and Intel® Integrated Sensor Solution on Skylake Mobile, Skylake Desktop, and Greenlow Workstation Platforms (CDI # 554868) for additional details.

CLSMNF = Close Manufacturing switch used with Intel® Flash Programming Tool (FPT)

PV = Production Version

For additional information on FPT see System Tools User Guide included with ME kit under system tools folder.

Table F-1. ISH Public Key Settings

Firmware	MCP	FPF Automatic Commit	FPF MEI command after CLSMNF (Yes/No)	FPF MEI command before CLSMNF (Yes/No)
Pre-production	Production	No	No - Not a valid combination	No - Not a valid combination
Production (PV not set)	Pre-production	No	Yes	No
Production (PV not set)	Production	No	Yes	No
Pre-production	Pre-production	No	Yes	No
Production (PV not set)	Production	Yes	No	No

Note: The Intel® FIT allows integration of binary files within Integrated Sensor Hub section under ISH Image and ISH Data. The Intel® FIT does not generate or create the required files. The table above lists configuration combinations that can be used. Please see VIP # 105658 - Intel® Integrated Sensor Solution 3.0 for SKL Program Alpha Corporate Milestone Release Version 3.0.0.1037 update for firmware information.